

32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology

Operating Conditions

- 2.0V to 3.6V, -40°C to +105°C, DC to 200 MHz
- 2.0V to 3.6V, -40°C to +125°C (Planned)

Core: 200 MHz / 330 DMIPS MIPS32® microAptiv™

- 32 KB I-Cache, 32 KB D-Cache
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
 - Four 64-bit accumulators
 - Single-cycle MAC, saturating and fractional math
- Code-efficient (C and Assembly) architecture

Clock Management

- Programmable PLLs and oscillator clock sources
- Dedicated PLL for DDR2
- Fail-Safe Clock Monitor
- Independent Watchdog and Deadman Timers
- Fast wake-up and start-up

Power Management

- Various power management options for extreme power reduction (VBAT, Deep Sleep, Sleep and Idle)
- Deep Sleep current: < 1 µA (typical)
- Integrated POR and BOR
- Programmable High/Low-Voltage Detect (HLVD) on VDD and High-Voltage Detect (HVD) on VDD1V8

Memory Interfaces

- DDR2 SDRAM interface (up to DDR 533)
- SD/SDIO/eMMC bus interface (up to 50 MHz)
- Serial Quad Interface (up to 80 MHz)
- External Bus Interface (up to 50 MHz)

Graphics Features

- 3-layer Graphics Controller with up to 24-bit color support
- High-performance 2D Graphics Processing Unit (GPU)

Audio Interfaces

- Audio data communication: I²S, LJ, and RJ
- Audio control interfaces: SPI and I²C
- Audio master clock: Fractional clock frequencies with USB synchronization

High-Speed Communication Interfaces (with Dedicated DMA)

- USB 2.0-compliant High-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features

- Crypto Engine with a RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
 - Peripheral and memory region access control

Direct Memory Access (DMA)

- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features

- 12-bit ADC modules:
 - 18 Msps with up to six ADC circuits (five dedicated and one shared)
 - Up to 45 analog inputs
 - Can operate during Sleep and Idle modes
 - Multiple trigger sources
 - Six Digital Comparators and six Digital Filters
- Two Comparators with 32 programmable voltage references
- Temperature sensor with ±2°C accuracy
- Charge Time Measurement Unit (CTMU)

Communication Interfaces

- Two CAN modules (with dedicated DMA channels):
 - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
 - Supports LIN 1.2 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as additional SPI module (up to 80 MHz)
- Five I²C modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Timers/Output Compare/Input Capture

- Nine 16-bit and up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

Input/Output

- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, and pull-downs
- Selectable slew rate control
- External interrupts on all I/O pins
- PPS to enable function remap

Qualification and Class B Support

- AEC-Q100 REVG (Grade 2 -40°C to +105°C)
- AEC-Q100 REVG (Grade 1 -40°C to +125°C) Planned
- Class B Safety Library, IEC 60730
- Back-up internal oscillator

Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Integrated Software Libraries and Tools

- C/C++ compiler with native DSP/fractional support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™, and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micrium® µC/OS™, and SEGGER embOS®

Packages

Type	LFBGA		LQFP
Pin Count	169	288	176
I/O Pins (up to)	120	120	120
Contact/Lead Pitch (mm)	0.8	0.8	0.4
Dimensions (mm)	11 x 11	15 x 15	20 x 20

PIC32MZ Graphics (DA) Family

TABLE 1: PIC32MZ DA FEATURES COMMON TO ALL DEVICES

Boot Flash Memory (KB)	Remappable Peripherals					12-bit ADC Channels	Analog Comparators	CTMU	USB 2.0 HS OTG	I ² C	GLCD	GPU	EBI	PMP	SQI	SDHC	RTCC	Ethernet	I/O Pins	JTAG	Trace
	Remappable Pins	Timers ⁽¹⁾ /Capture/Compare	UART	SPI/I ² S	CAN 2.0B	External Interrupts ⁽²⁾															
64	47	9/9/9	6	6	2	5	45	2	Y	Y	5	Y	Y	Y	Y	Y	Y	Y	120	Y	Y

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

TABLE 2: 169-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/Dedicated)
PIC32MZ1025DAA169	1024	256	No	—	N	8/24
PIC32MZ1025DAB169					Y	8/26
PIC32MZ1064DAA169		640			N	8/24
PIC32MZ1064DAB169					Y	8/26
PIC32MZ2025DAA169	2048	256			N	8/24
PIC32MZ2025DAB169					Y	8/26
PIC32MZ2064DAA169		640			N	8/24
PIC32MZ2064DAB169					Y	8/26
PIC32MZ1025DAG169	1024	256	Yes (INT)	32	N	8/24
PIC32MZ1025DAH169					Y	8/26
PIC32MZ1064DAG169		640			N	8/24
PIC32MZ1064DAH169					Y	8/26
PIC32MZ2025DAG169	2048	256			N	8/24
PIC32MZ2025DAH169					Y	8/26
PIC32MZ2064DAG169		640			N	8/24
PIC32MZ2064DAH169					Y	8/26

TABLE 3: 176-PIN LQFP PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (programmable/Dedicated)
PIC32MZ1025DAA176	1024	256	No	—	N	8/24
PIC32MZ1025DAB176		640			Y	8/26
PIC32MZ1064DAA176					N	8/24
PIC32MZ1064DAB176					Y	8/26
PIC32MZ2025DAA176	2048				256	N
PIC32MZ2025DAB176		640			Y	8/26
PIC32MZ2064DAA176					N	8/24
PIC32MZ2064DAB176					Y	8/26
PIC32MZ1025DAG176	1024		256	Yes (INT)	32	N
PIC32MZ1025DAH176		640	Y			8/26
PIC32MZ1064DAG176			N			8/24
PIC32MZ1064DAH176			Y			8/26
PIC32MZ2025DAG176	2048		256			N
PIC32MZ2025DAH176		640	Y			8/26
PIC32MZ2064DAG176			N			8/24
PIC32MZ2064DAH176			Y			8/26

TABLE 4: 288-PIN LFBGA PIC32MZ DA FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal/External)	Crypto/RNG	DMA Channels (Programmable/Dedicated)
PIC32MZ1025DAA288	1024	256	Yes (EXT)	N	8/24
PIC32MZ1025DAB288		640		Y	8/26
PIC32MZ1064DAA288				N	8/24
PIC32MZ1064DAB288				Y	8/26
PIC32MZ2025DAA288	2048			256	N
PIC32MZ2025DAB288		640		Y	8/26
PIC32MZ2064DAA288				N	8/24
PIC32MZ2064DAB288				Y	8/26