AN 583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs

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This application note provides guidelines for designing ferrite bead filter networks to isolate shared power rails of Stratix® IV FPGAs.

Advancements in FPGA technology have increased data rates beyond 10 Gbps. To achieve these data rates, FPGA manufacturers typically require multiple isolated digital and analog supply rails to separately power the core and I/Os as well as the sensitive phase-locked loops (PLLs) and gigabit transceiver blocks within the FPGA. As a result, the complexity of the power distribution system on the board is greatly increased.

With limited board space, layer count, and cost budgets, board designers are finding it increasingly challenging to design their FPGA boards within the constraints of their system requirements. One way to simplify this power design for the Stratix IV GX and GT family of multi-gigabit transceiver-based FPGAs is to be able to cleanly share similar voltage rails while maintaining adequate high-frequency separation between the shared rails. A common strategy is to use ferrite beads.

This application note describes proper bead selection and design considerations such as anti-resonance, inductor-capacitor (LC) tank oscillation avoidance, transfer impedance analysis, and DC voltage (IR) drop minimization, while meeting target impedance requirements for decoupling. Also described is an alternative method of using a PCB layout structure to replace the ferrite bead as the inductive filter component in some instances. Simulation results comparing the performance of the PCB structure to the ferrite bead are evaluated to validate the effectiveness of the PCB structure filter network and to understand its limitations.

Ferrite Bead Selection

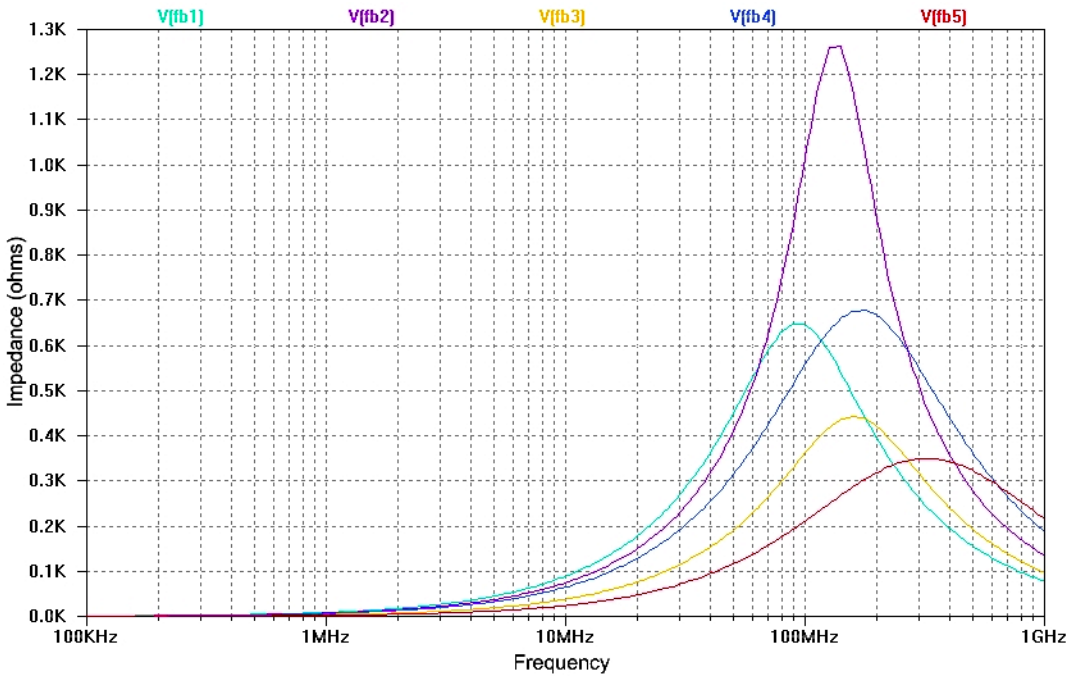
Generally, ferrite beads fall into two categories[1]:

- High-Q Beads—Typically used as resonators and must not be used in power isolation circuits.
- Low-Q Beads—Also known as absorptive beads, are more lossy and make good power filter networks because they are designed to absorb high-frequency noise currents and dissipate it as heat. These beads have high impedance over wide high-frequency bands, making them ideal as low-pass noise filters.

Manufacturers typically specify the characteristic performance of their ferrite beads in terms of an impedance-versus-frequency plot as well as providing the maximum DC current and DC resistance rating. Depending on the design of the bead and the material used, the impedance plot can vary significantly in magnitude across a broad frequency spectrum, making proper bead selection confusing.

Figure 1 shows an example of five ferrite bead impedance curves plotted together across a 1 GHz frequency range to compare the performance of various low-Q beads that you can use for power supply noise filtering[2].

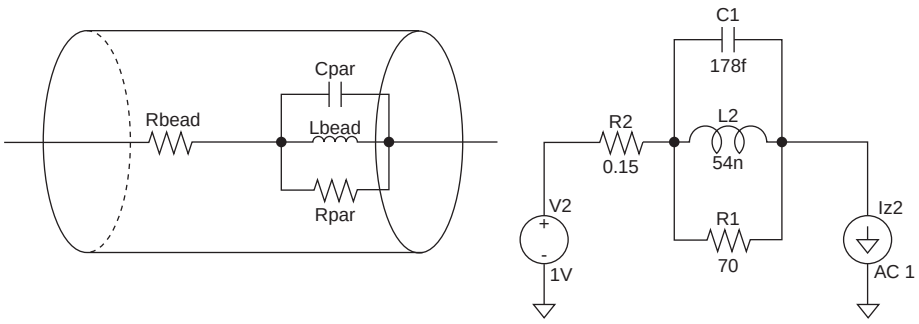
Figure 1. Comparison of Five Ferrite Bead Impedance Plots



Ferrite Bead Modeling and Simulation

Bead manufacturers usually provide equivalent SPICE circuit models for their devices for system simulation. However, in the event that a bead model is not readily available from the manufacturer, a ferrite bead can be modeled as a simple network of R, L, and C components, as shown in Figure 2 (left)[3].

Figure 2. Ferrite Bead Circuit Model (Left) and SPICE Simulation Setup (Right)



Although the model is a first-order approximation, you can still use it effectively for sub-GHz simulations.

- R_{bead} and L_{bead} are the DC resistance and effective inductance of the bead.
- C_{par} and R_{par} are the parallel capacitance and resistance associated with the bead.

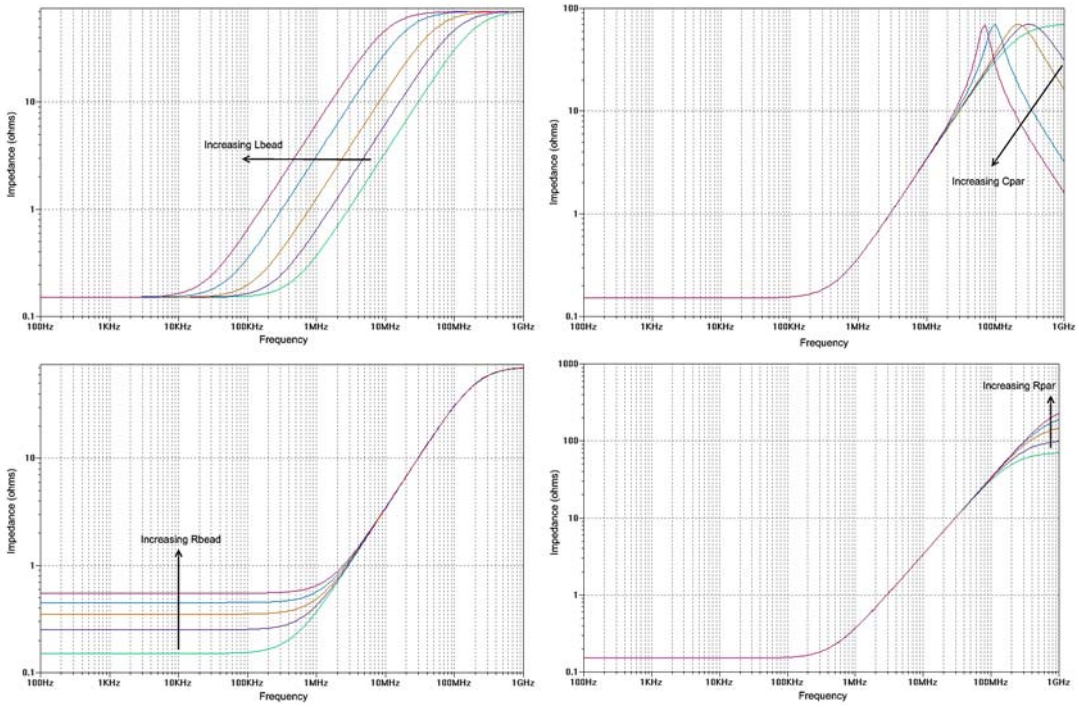
At low frequencies, C_{par} is an open circuit and L_{bead} is a short circuit, leaving only R_{bead} as the DC resistance of the bead. As frequency increases, the impedance of L_{bead} starts to increase linearly with frequency ($j\omega L_{bead}$) while the impedance of C_{par} decreases inversely proportionally to frequency ($1/j\omega C_{par}$). The rising linear slope of the bead's impedance-versus-frequency plot is determined mainly by the inductance of L_{bead}.

At a certain high frequency point, the impedance of C_{par} begins to dominate and the bead's impedance starts to decrease, countering its inductance. In this case, the falling slope of the impedance-versus-frequency plot is determined mainly by the parasitic capacitance C_{par} of the bead. R_{par} helps to dampen the Q-factor of the bead. However, too large of R_{par} and C_{par} values increases the Q-factor of the bead and decreases its effective bandwidth. This can result in a high-Q bead that causes unwanted ringing in the transient response of the power distribution network (PDN).

To observe how each of these parameters affects the beads' frequency response, you can use SPICE to simulate the AC response of a bead in isolation. Figure 2 (right) shows the SPICE circuit setup for obtaining the AC response of a sample ferrite bead that has a DC resistance of 0.15 Ω, an effective inductance of 54nH, and a parallel capacitance and resistance of 178fF and 70 Ω, respectively.

Figure 3 shows this bead's characteristic impedance-versus-frequency plot when a 1 V source and 1A AC current load is applied with an AC analysis sweep from 100 Hz to 1 GHz in SPICE. By varying each R, L, and C component individually in the simulation, the SPICE model can be curve-fitted to approximate a specific ferrite bead when the manufacturer does not provide a SPICE model.

Figure 3. Effect of Varying R, L, and C

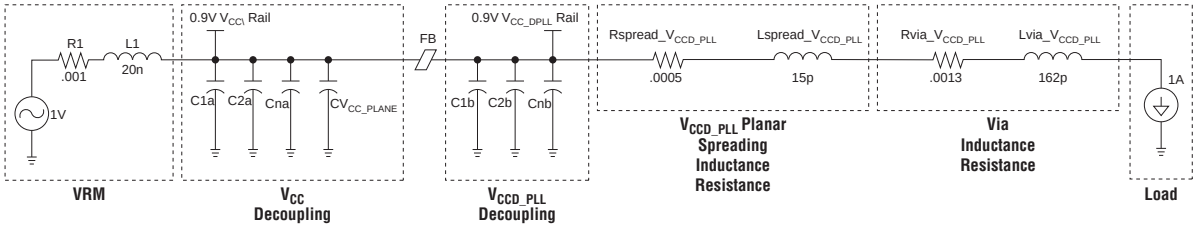


Stratix IV GX Design Example

For many applications, high-speed clocks, data, and other I/O switching rates can range from hundreds of megahertz up to the multi-gigahertz. The fundamental frequency and harmonics associated with each of these switching signals can easily pollute sensitive power rails, causing increased voltage ripple and output jitter, especially if they are shared with other noisy digital rails. For example, in Stratix IV GX devices, the 0.9 V V_{CC} (core) voltage is used to power the noisy digital logic elements (LEs), memory elements, and DSP blocks, among others, within the FPGA fabric. On the other hand, the 0.9 V V_{CCD_PLL} is used to power the more sensitive PLLs used for the clock multipliers. While it is simple to combine the V_{CC} with the V_{CCD_PLL} rail to a single voltage plane on the PCB (powered by a single voltage regulator source), doing so can allow core-coupled noise to negatively impact the PLLs performance. A better solution is to use a ferrite bead between the V_{CC} and V_{CCD_PLL} rails with the appropriate decoupling capacitors chosen for each rail to meet their respective target impedances.

Figure 4 shows a design example for the Stratix IV EP4SGX230KF40 device where the V_{CC} and V_{CCD_PLL} are isolated using a ferrite bead. In this example, the ferrite bead chosen is a Laird Technologies LI0805H121R-10.

Figure 4. Stratix IV GX V_{CC} to V_{CC_PLL} Design Example



The decoupling for the V_{CC} rail (denoted by C1a and C2a to C*n*a) is designed to meet an impedance target of 9 mΩ until 25 MHz using Altera's PowerPlay Early Power Estimator (EPE) and PDN decoupling tool. Similarly, the V_{CCD_PLL} decoupling (denoted by C1b and C2b to C*n*b) is designed for 0.45 Ω target impedance until at least 70 MHz using the same target impedance methodology.

For more information about using the PowerPlay EPE and PDN tools, and applying the target impedance method for decoupling, refer to the following information:

- PowerPlay Early Power Estimators (EPE) and Power Analyzer
- Power Distribution Network Design Tool for Stratix IV Devices
- Board Design Resource Center
- *AN 574: Printed Circuit Board (PCB) Power Delivery Network (PDN) Design Methodology*

Table 1 summarizes the required decoupling capacitances for each rail to meet its respective impedance targets when using the PDN decoupling tool. Planar spreading resistance and inductance, as well as BGA via resistance and inductance estimated by the PDN tool, are also included in the SPICE deck to give a complete PDN profile extending up to the BGA ball of the device.

For the complete SPICE deck for obtaining the PDN profile of this V_{CC} to V_{CCD_PLL} example, refer to the *VCC to VCCDPLL Z Profile Example* found in *AN 583: VCC to VCCDPLL Spice Examples.zip*.

Table 1. Decoupling Capacitors from the PDN Tool (Part 1 of 2)

V_{CC} Rail			V_{CCD_PLL} Rail		
Capacitor	**Value (µF)**	**Quantity**	**Capacitor**	**Value (µF)**	**Quantity**
C1a - C7a	330	7	C1b - C2b	4.70	2
C8a - C12a	2.20	5	—	—	—
C13a - C14a	0.47	2	—	—	—
C15a - C18a	0.22	4	—	—	—

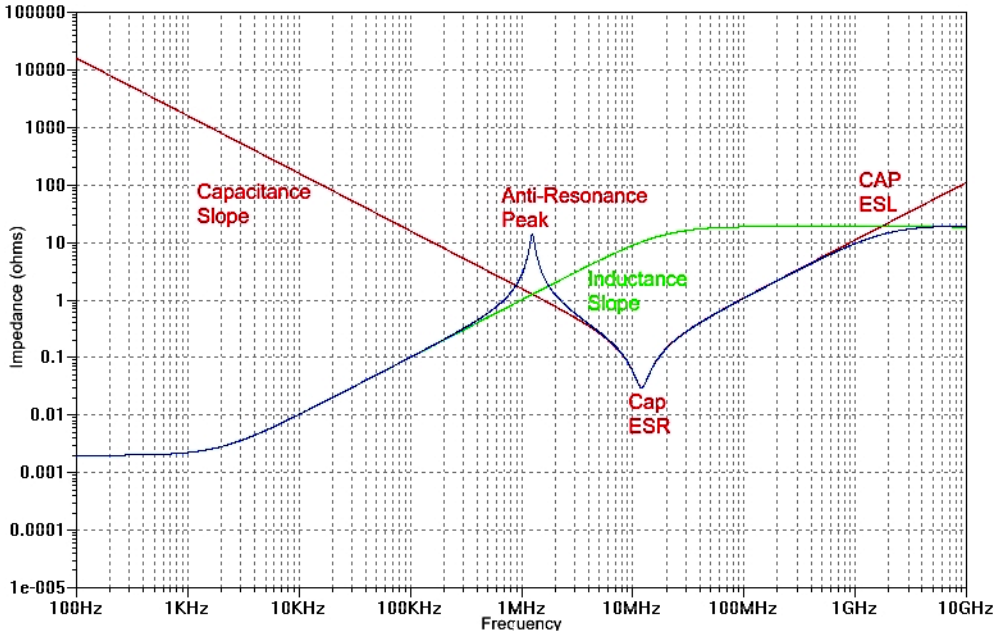
Table 1. Decoupling Capacitors from the PDN Tool (Part 2 of 2)

V_{CC} Rail			V_{CCD_PLL} Rail		
Capacitor	**Value (μF)**	**Quantity**	**Capacitor**	**Value (μF)**	**Quantity**
C19a - C23a	0.10	5	—	—	—
C24a - C37a	0.047	14	—	—	—

Anti-Resonance

When implementing a ferrite bead, be aware of possible anti-resonance peaks that may cause the resulting impedance profile to violate the target impedance limit. These anti-resonance peaks can occur whenever a falling capacitance slope intersects with the rising inductance slope of the bead, as shown in Figure 5.

Figure 5. Cause of Anti-Resonance Spike



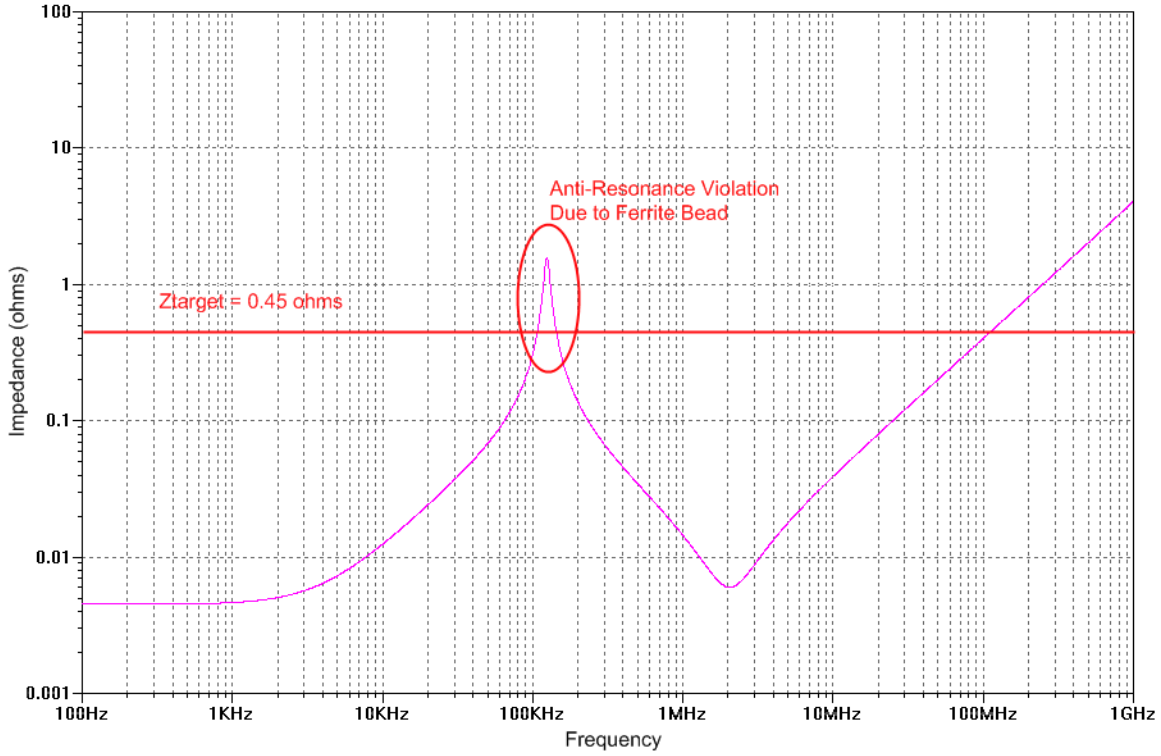
If the target impedance is low, these peaks can easily violate the target impedance limit. Use SPICE or a similar circuit simulator to ensure these anti-resonance peaks do not violate the target impedance.

For the Stratix IV GX V_{CC} to V_{CCD_PLL} isolation example above, the PDN tool does not account for the effects of the ferrite bead. Therefore, SPICE is used to verify that the inclusion of the bead does not alter the PDN profile by introducing an unwanted anti-resonance.

With SPICE, a unit voltage regulator source, modeled as a simple series connected resistor-inductor network driving a 1A load, is placed across the PDN circuit being modeled. The circuit is then stimulated with an AC sweep from 100 Hz to 1 GHz to obtain the resulting impedance profile of the decoupling network in Ω. As shown in Figure 6, the decoupling capacitors for the V_{CCD_PLL} rail estimated by the PDN tool, together with the chosen Laird Technologies LI0805H121R-10 ferrite bead, causes a severe anti-resonance spike of approximately 1.5 Ω at 124 KHz. This violates the V_{CCD_PLL} impedance target of 0.45 Ω and must be resolved.

For the complete SPICE deck for obtaining the PDN profile of this V_{CC} to V_{CCD_PLL} example with the effects of the ferrite bead included, refer to the *VCC to VCCDPLL Bead Anti Resonance Example* found in *AN 583: VCC to VCCDPLL Spice Examples.zip*.

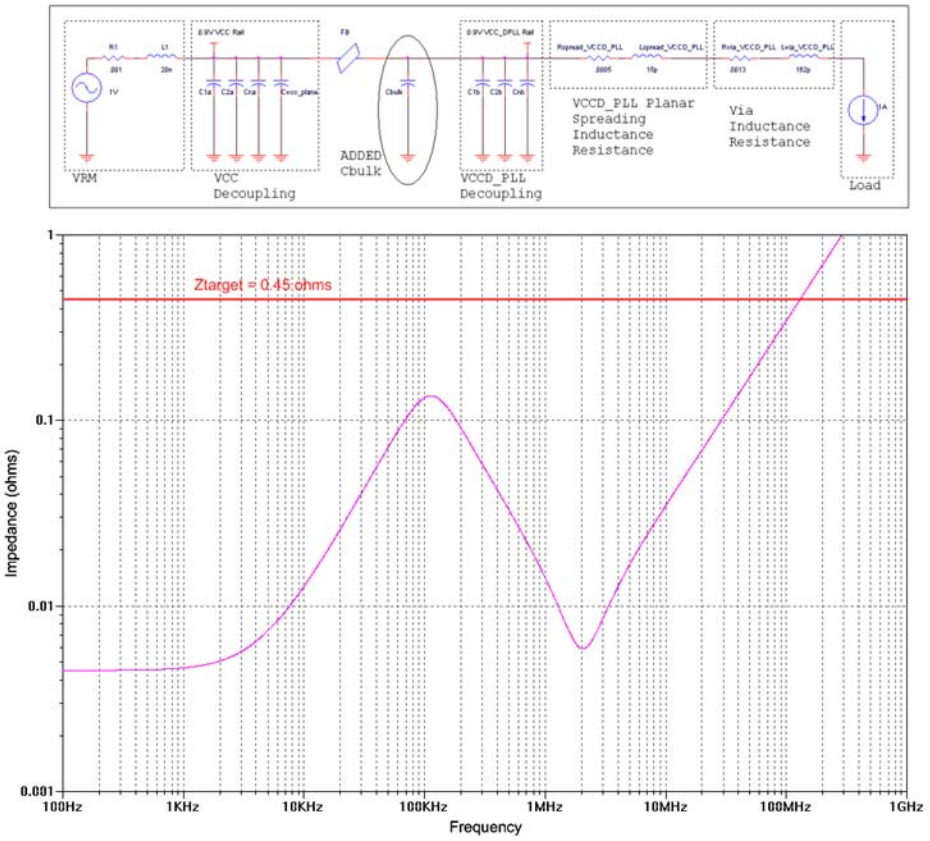
Figure 6. Anti-Resonance Spike Violation Example



To defeat this low frequency anti-resonance spike, add a large bulk decoupling capacitor to the V_{CCD_PLL} as shown in Figure 7 (top). Figure 7 (bottom) shows the resulting PDN profile when a 47 µF bulk capacitor is added to the V_{CCD_PLL} rail. The additional bulk capacitance helps mitigate this anti-resonance violation.

For the complete SPICE deck for obtaining the PDN profile of this V_{CC} to V_{CCD_PLL} example with the addition of the bulk decoupling capacitor, refer to the *VCC to VCCDPLL Bulk Cap Mitigation Example* found in *AN 583: VCC to VCCDPLL Spice Examples.zip*.

Figure 7. PDN Circuit with Added 47 µF Capacitor (Top) and Simulation Result (Bottom)



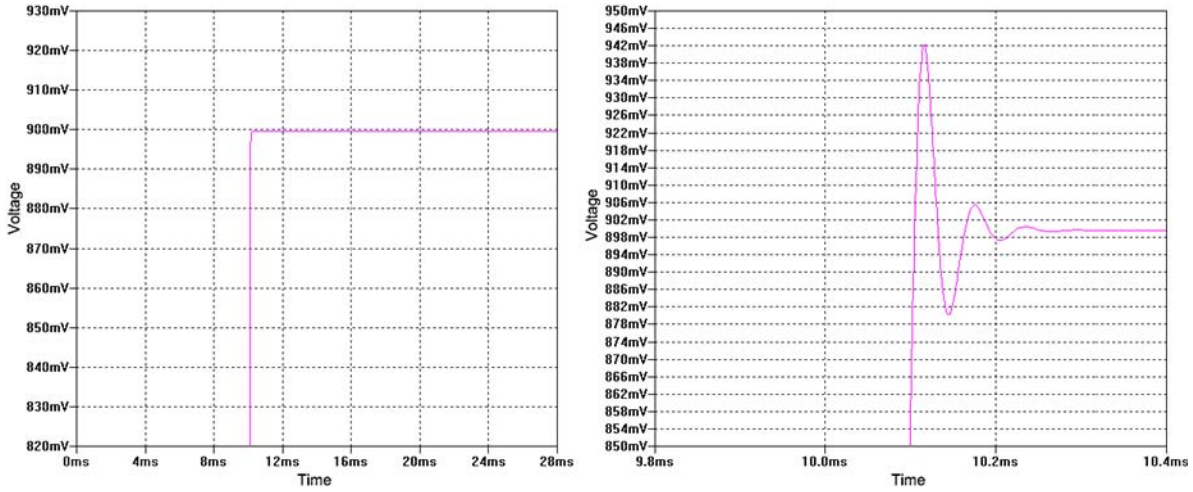
LC Tank Oscillations

Another concern when using ferrite beads is LC tank oscillation. Whenever you use inductors and capacitors in a PDN circuit, the energy stored in the inductor and capacitor sloshes back and forth between these two energy storage elements, causing possible unwanted circuit oscillations. This adverse effect is observed in the time domain as voltage overshoot or even ringing.

Use a SPICE simulator or similar tool with a transient analysis to verify that any overshoot or ringing is well damped and within acceptable limits for your design. In the previous Stratix IV GX V_{CC} to V_{CCD_PLL} example, the Laird Technologies LI0805H121R-10 ferrite bead did not cause voltage overshoot or ringing, as shown in Figure 8 (left). If overshoot or ringing did occur, ensure that it is still within the ±30 mV operating specifications for the 0.9 V V_{CCD_PLL} rail. Usually, if the inductance of the bead is much higher, as in the hypothetical situation of Figure 8 (right), the overshoot and ringing can be more severe, leading to failures or incorrect operation of the device. If severe overshoot or ringing occurs, select a different ferrite bead with a lower inductance value.

For the complete SPICE deck for obtaining the transient analysis of this V_{CC} to V_{CCD_PLL} overshoot example, refer to the *VCC to VCCDPLL Transient Response Example* found in *AN 583: VCC to VCCDPLL Spice Examples.zip*.

Figure 8. PDN Critically Damped Response (Left) and Severe Overshoot and Ringing (Right)



Transfer Impedance

A common method for evaluating the noise immunity of a circuit is to analyze its transfer impedance. To determine the transfer impedance of the V_{CC} to V_{CCD_PLL} isolation for the example above, you can simulate the PDN circuit from the V_{CC} side of the bead with a 1A current source to emulate noise coming from the V_{CC} rail within the FPGA device, as shown in Figure 9.

Figure 9. V_{CC} to V_{CCD_PLL} Transfer Impedance Circuit

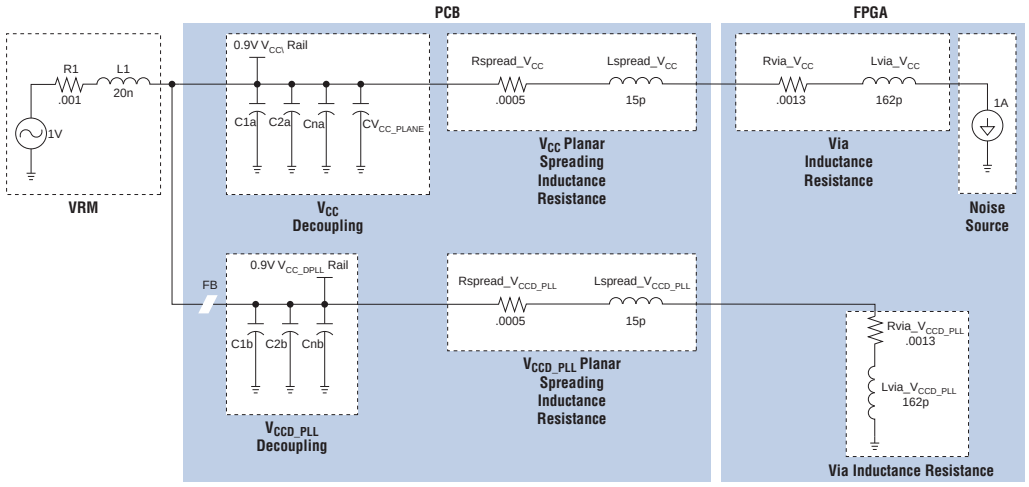
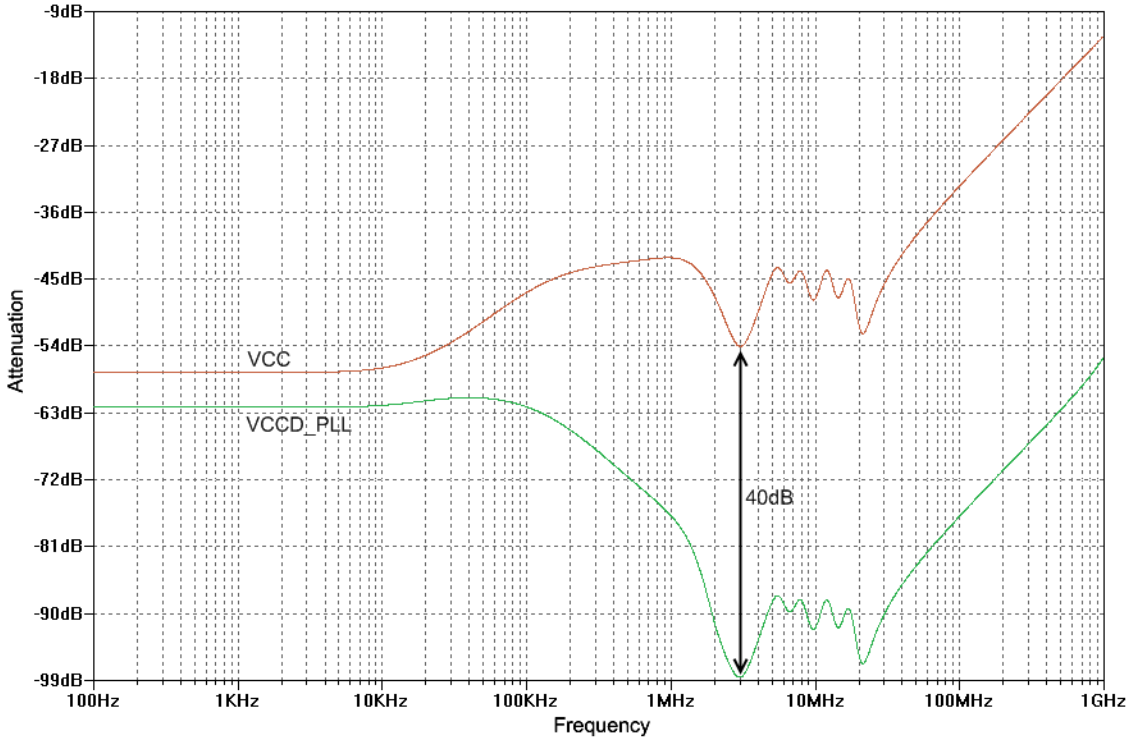


Figure 10 shows the resulting transfer impedance of the V_{CC} rail just before the ferrite bead and the isolated V_{CCD_PLL} rail at the BGA Ball of the FPGA device. The V_{CCD_PLL} is lower than the V_{CC} by approximately 40 dB from 3 MHz and beyond, due to the isolation from the ferrite bead and the V_{CCD_PLL} decoupling network.

For the complete SPICE deck of the transfer impedance of this V_{CC} to V_{CCD_PLL} isolation example, refer to the *VCC to VCCDPLL Transfer Z Isolation Example* found in *AN 583: VCC to VCCDPLL Spice Examples.zip*.

Figure 10. Transfer Impedance



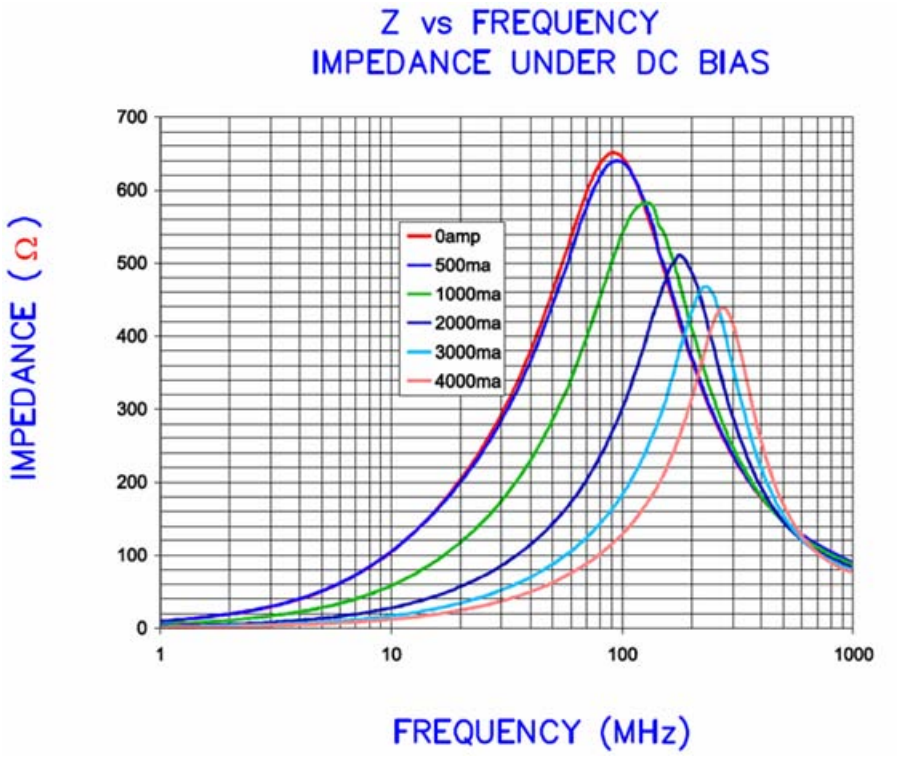
Although the examples presented in this application note are specific to the V_{CCD_PLL} rail, other rails of Stratix IV GX and GT devices, such as V_{CCL_GXB}, V_{CCAUX}, and V_{CCA}, can also benefit from the same isolation technique and analysis described.

DC Current and IR Drop Considerations

The amount of current that the bead can pass is determined by its maximum DC current rating as specified in its datasheet. Exceeding this maximum current rating can damage the bead. However, even current levels below the maximum rated DC value can cause the bead to significantly lose its effectiveness as the core material of the bead becomes saturated.

Figure 11 shows an example impedance-versus-frequency curve for a ferrite bead under varying DC current bias conditions(4). As current flow increases through the bead, the effective impedance and bandwidth of the bead decreases.

Figure 11. Impedance Curve with DC Bias *(Note 1)*



Note to Figure 11:

(1) Reprinted with permission, courtesy of Laird Technologies.

To avoid core saturation and degradation of the bead's performance, select the ferrite bead with a DC current rating of more than twice that of the required current of the target rail. Also, select a low DC resistance bead to minimize the associated DC IR drop. Verify that any voltage drop does not cause the target supply rail to fall below the recommended operating conditions of the FPGA, as specified in the device datasheet.

PCB Structures

An alternate method to using a ferrite bead is to construct a small inductive PCB layout structure for connecting the two isolated power planes. This method requires careful modeling and extraction of the DC resistance and AC loop inductance associated with the PCB structure, as well as SPICE simulations to verify the structures filter performance in place of the ferrite bead. The DC resistance determines the voltage drop caused by the trace length of the structure. The AC loop inductance helps provide isolation for the two connecting power rails.

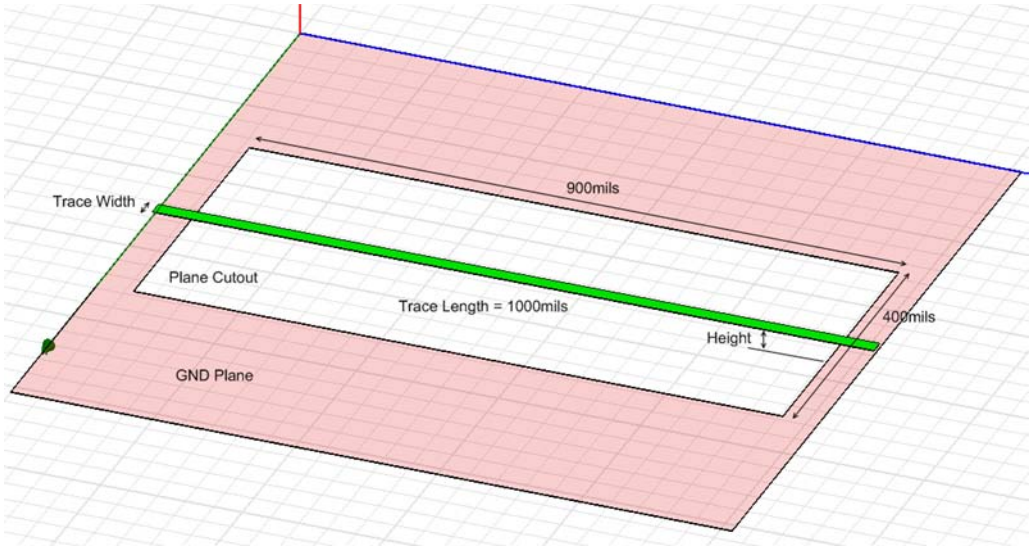
In the following examples, Altera used Ansoft Q3D Extraction software to model, evaluate, and tune several PCB structures that work well for isolating the Stratix IV GX V_{CC} and V_{CCD_PLL} rails. With Q3D, the DC resistance and AC loop inductance for each structure is extracted. These values are then re-simulated in SPICE to validate the structures performance in comparison with the performance of the ferrite bead simulated previously.

Example 1: Straight Trace Structure

In the straight trace construction shown in Figure 12, a 20 mil wide, 1 oz copper power trace is used in place of the ferrite bead to connect the two power planes under consideration. A trace of this construction can carry approximately 3.7 A of current[5]. You must design the trace to handle the expected current load. The parameters that directly affect the inductance of the trace are primarily the length of the trace, its height from the reference plane, and the size of the cutout area underneath the trace.

In general, the longer the trace length, the further the trace is away from the reference plane, or the larger the plane cutout area, all work to increase the resultant trace inductance due to the larger return current loop area created. However, making each of these parameters too large consumes precious board real estate. A better topology is to use a coiled trace approach.

Figure 12. Straight Trace Structure



Example 2: Coil Trace Structure

To minimize board space usage while maximizing trace loop inductance, use a coil trace structure, as shown in Figure 13. Because the current flow in the coil is always in the same direction along any parallel segment of the coil, no current cancellation occurs and the maximum inductance is achieved in a small area. However, using the coil structure requires an escape via for the trace to exit on a different layer. Because of this, consider the current handling of the via. In general, a single 12 mil diameter via with a 1 mil wall plating can pass approximately 2.5 A of current[5].

Figure 13. Coil Trace Structure

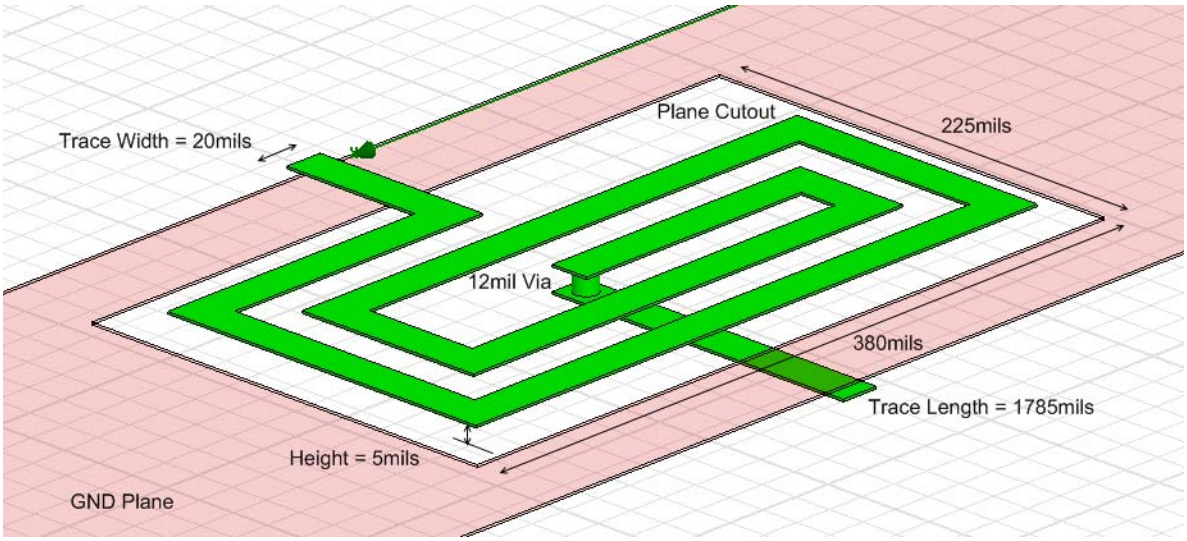


Table 2 shows the effect on the DC resistance and trace inductance for different cases of straight and coiled trace lengths, height from the reference plane, and size of the plane cutout area for reference as extracted by Q3D. The DC resistance is mainly dependent on the length of the trace for a given trace width, as shown in Table 2.

Table 2. Comparison of AC Loop Inductance

Case	Description	Length (mils)	Height (mils)	Plane Cutout (Xmils × Ymils)	DCR (mΩ)	Inductance (nH)
1	Short straight trace with no cutout	250	2.7	None	7	3.8
2	Long straight trace with no cutout	1000	2.7	None	29	9.1
3	Long straight trace with increased height and no cutout	1000	5	None	29	17.5
4	Long straight trace with increased height and a small cutout	1000	5	400 × 900	29	22.4
5	Long straight trace with increased height and a large cutout	1000	5	800 × 900	31	26.1
6	Coiled trace with a cutout	1785	5	225 × 380	48	26.8

Simulation Results

Using the Q3D extracted DC resistance of 48 mΩ and the AC loop inductance of 26.8 nH from the coil structure, and re-simulating these values in the previous V_{CC} to V_{CCD_PLL} SPICE examples, gives the following results for the impedance profile (Figure 14), transfer impedance (Figure 15), and transient response (Figure 16). The three figures show that you can use the coiled PCB layout structure in place of the ferrite bead if the DC voltage drop across the structure is maintained within the recommended operating conditions of the device as specified in the datasheet.

Figure 14. Impedance Profile with Coil Structure

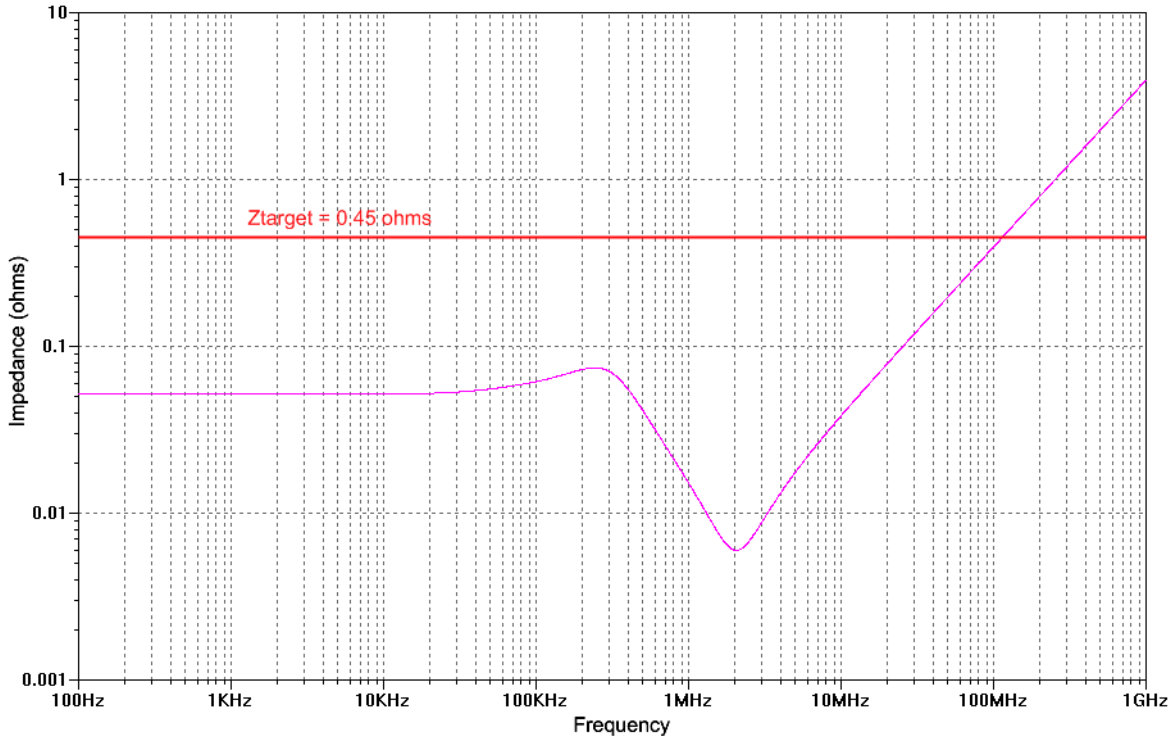


Figure 15. Transfer Impedance Profile with Coil Structure

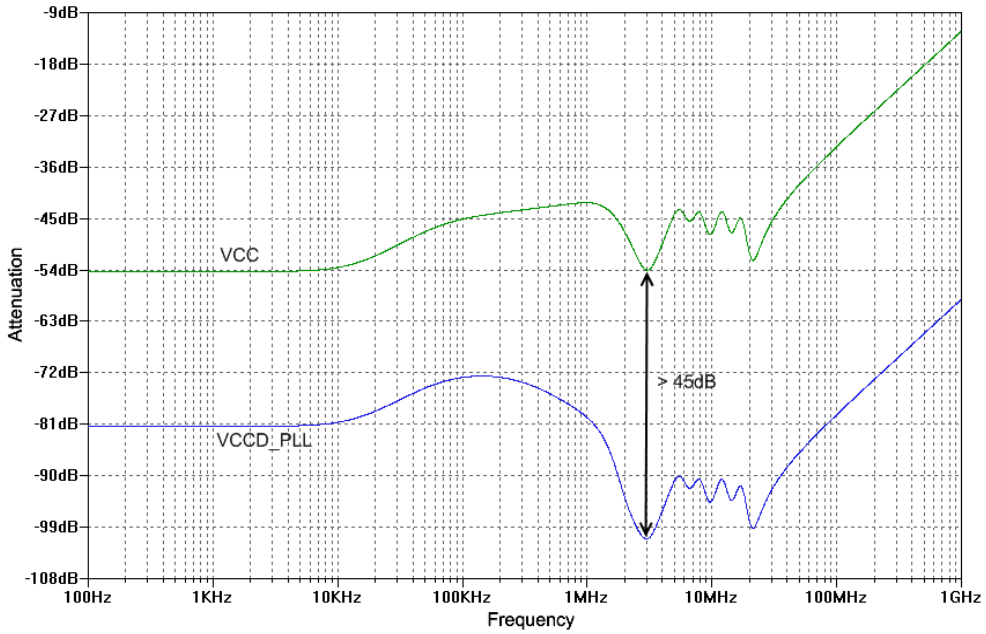
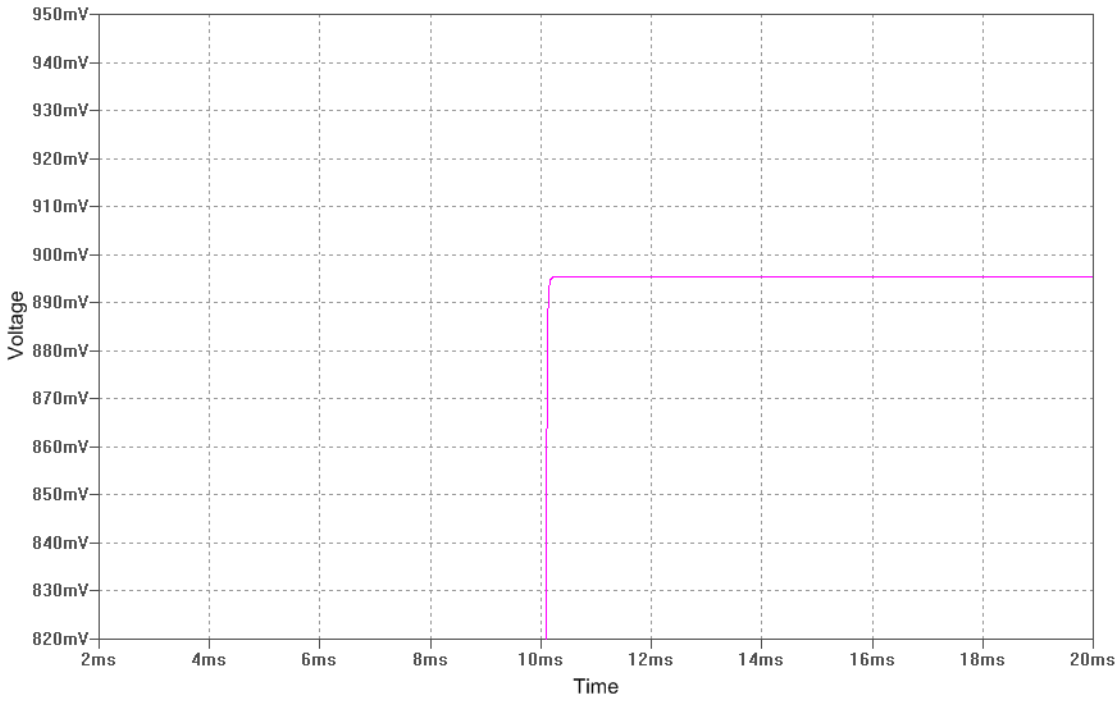


Figure 16. Transient Response with Coil Structure



EMC Compliance

These structures can be a source of strong radiated emissions that may impact Electro-Magnetic Compliance (EMC) regulations imposed by the Federal Communication Commission (FCC) and other international regulatory agencies. Sandwiching the structure between ground planes stitched together with vias helps shield any radiated emissions. Additional EMC compliance simulation and testing of these structures has not been performed by Altera and is beyond the scope of the application note.

Design Recommendations

Altera recommends the following for your design:

- Select a ferrite bead or design the PCB filter structure such that it can pass the required current load expected by the filtered rail.
  - To avoid core saturation, select a ferrite bead with a current rating of at least twice that of the expected current for the target voltage rail.
  - Minimize the DC resistance of the bead or PCB structure to reduce the DC IR drop.
  - Verify that any voltage drop does not cause the target supply rail to fall below the recommended operating conditions of the device.
- Use SPICE or another similar tool to ensure any anti-resonance peaks caused by the ferrite or PCB inductive structure does not violate the target impedance limit.
  - If an anti-resonance violation occurs, add additional bulk decoupling capacitors to the filtered rail to reduce or eliminate the spike.
- Use SPICE or another similar tool to analyze the transient response of the PDN circuit for excessive voltage overshoot or ringing that may violate the device recommended operating conditions.
- Use SPICE or another similar tool to analyze the transfer impedance of the isolated voltage rail versus the unfiltered parent rail for adequate attenuation.

Conclusion

The Stratix IV GX and GT family of high-performance FPGAs require multiple supply rails to power the various circuit blocks within the device. In order for the device to achieve its maximum rated performance with minimal jitter, certain sensitive supply rails require very clean power sources. To meet these power demands within system design constraints, you can use ferrite beads or custom PCB structures as the filter element to isolate some shared supply rails. This applications note shows how to select the appropriate ferrite bead and design the PCB structure to meet the power filter requirements for a Stratix IV GX- and GT-based PDN design.

References

1. *Ferrite Beads*, EDN Article, October 12, 2000, Howard Johnson, Phd.
2. Five Laird Technologies, ferrite beads are plotted for comparison:
   - HI2220P601R-10
   - MI0805J102R-10
   - MI1206L391R-10
   - MI0603J601R-10
   - MI0603L301R-10
3. Ferrite bead model extrapolated from LTSpice, www.linear.com.
4. Laird Technologies, Steward HI2220P601R-10 ferrite bead datasheet.
5. Saturn PCB Design Reference Toolkit v3.9, www.saturnpcb.com.

Document Revision History

Table 3 shows the revision history for this application note.

Table 3. Template Revision History

Date and Revision	Changes Made	Summary of Changes
July 2009	Initial release.	—

101 Innovation Drive
San Jose, CA 95134
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Technical Support
www.altera.com/support