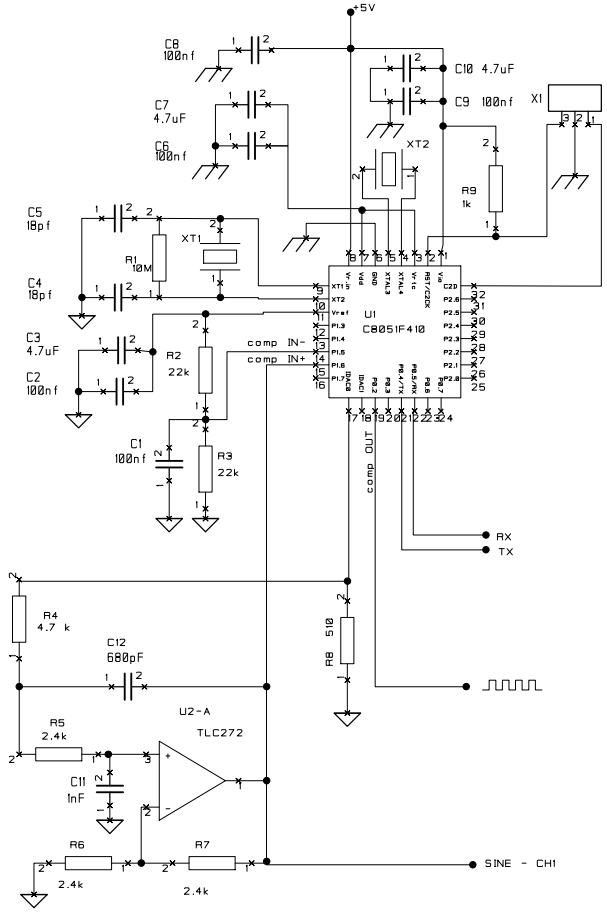
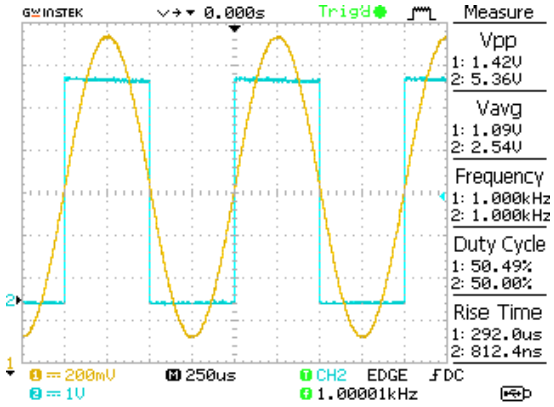


C8051F410 clock - 50 MHz
DDS loop - 40 ticks
Phase Accumulator 32 bit
sine table width - 9 bit

DAC sampling F - 1.25 MHz
DAC full scale 2 mA
DAC midscale code 2048
DAC max code 3496
DAC min code 600
Offset + 0x0A00

LPF cut off F - 60kHz



CONTRACT NO.		COMPANY NAME Zuken	
APPROVALS	DATE	DWG B-Size Sheet	
DRAWN		SIZE B	FSCM NO. / DWG NO. / REV.
CHECKED			
ISSUED		SCALE	SHEET 1 of 1