

DESCRIPTION

The M37516F8HP is the 8-bit microcomputer based on the 740 family core technology.

The M37516F8HP is designed for household products and office automation equipment and includes serial I/O functions, 8-bit timer, A-D converter, and I²C-BUS interface.

FEATURES

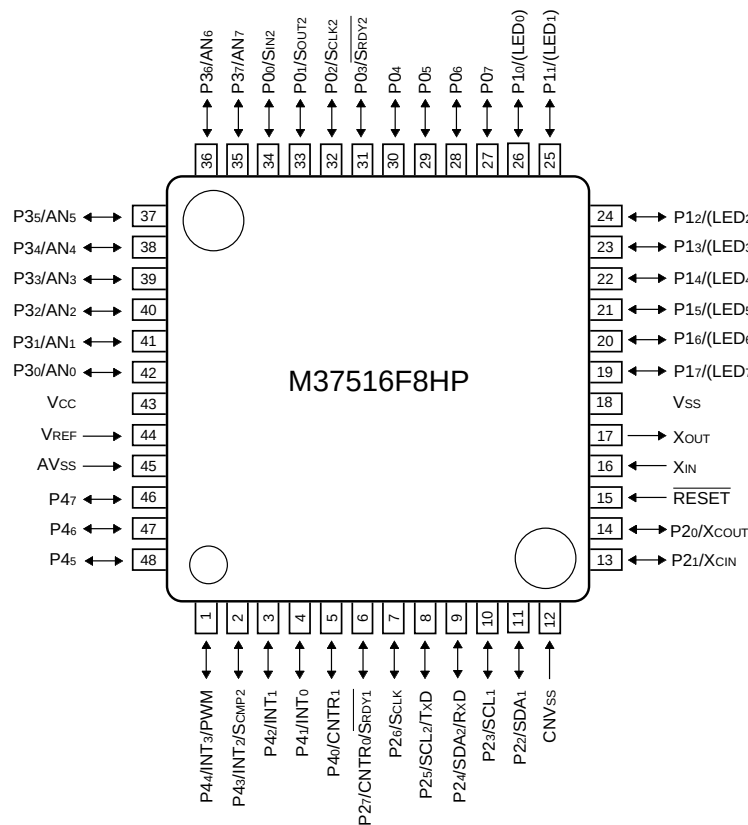
- Basic machine-language instructions 71
- Minimum instruction execution time 0.5 μ s
 (at 8 MHz oscillation frequency)
- Memory size
 Flash memory 32 Kbytes
 RAM 1 Kbytes
- Programmable input/output ports 40
- Interrupts 17 sources, 16 vectors
- Timers 8-bit X 4
- Serial I/O1 8-bit X 1 (UART or Clock-synchronized)
- Serial I/O2 8-bit X 1 (Clock-synchronized)
- Multi-master I²C-BUS interface (option) 1 channel
- PWM 8-bit X 1
- A-D converter 10-bit X 8 channels
- Watchdog timer 16-bit X 1

- Clock generating circuit Built-in 2 circuits
 (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
 In high-speed mode 4.0 to 5.5 V
 (at 8 MHz oscillation frequency)
 In high-speed mode 2.7 to 5.5 V
 (at 4 MHz oscillation frequency)
 In middle-speed mode 2.7 to 5.5 V
 (at 8 MHz oscillation frequency)
 In low-speed mode 2.7 to 5.5 V
 (at 32 kHz oscillation frequency)
- Power dissipation
 In high-speed mode 34 mW
 (at 8 MHz oscillation frequency, at 5 V power source voltage)
 In low-speed mode T.B.D.
 (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range -20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 48P6Q-A

Fig. 1 M37516F8HP pin configuration

FUNCTIONAL BLOCK

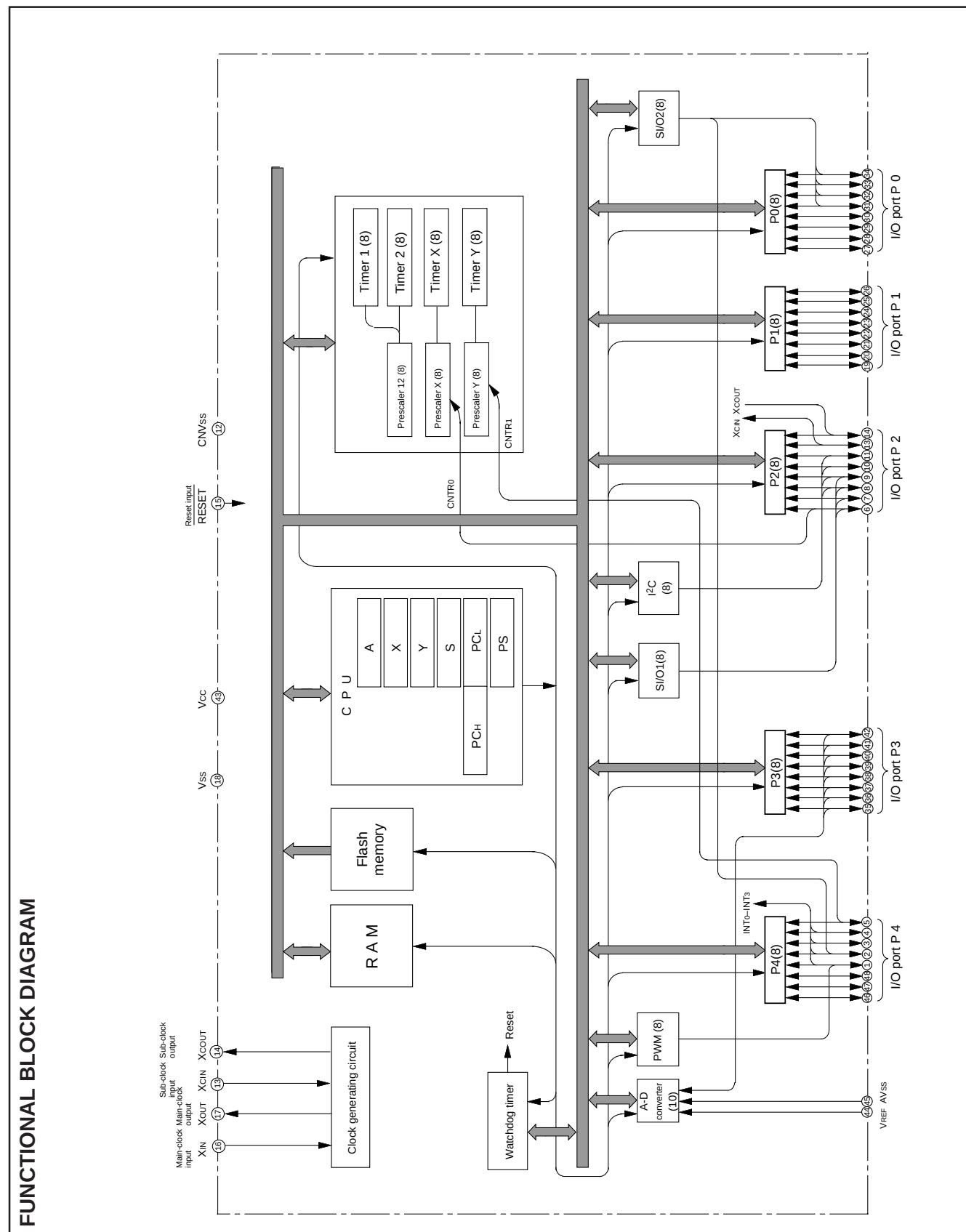


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	
			Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVSS	CNVss input	•This pin controls the operation mode of the chip. •Normally connected to Vss.	
RESET	Reset input	•Reset input pin for active “L.”	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.	
XOUT	Clock output	•When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2 P04–P07	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure.	• Serial I/O2 function pin
P10–P17		•P10 to P17 (8 bits) are enabled to output large current for LED drive.	
P20/XCOUT P21/XCIN P22/SDA1 P23/SCL1 P24/SDA2/RxD P25/SCL2/TxD P26/SCLK P27/CNTR0/ SRDY1	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •P22 to P25 can be switched between CMOS compatible input level or SMBUS input level in the I ² C-BUS interface function. •P20, P21, P24 to P27: CMOS3-state output structure. •P24, P25: N-channel open-drain structure in the I ² C-BUS interface function. •P22, P23: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonator) • I ² C-BUS interface function pins
			• I ² C-BUS interface function pin/ Serial I/O1 function pins
			• Serial I/O1 function pin
			• Serial I/O1 function pin/ Timer X function pin
P30/AN0– P37/AN7	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
P40/CNTR1 P41/INT0 P42/INT1 P43/INT2/SCMP2 P44/INT3/PWM P45–P47	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin • Interrupt input pins
			• Interrupt input pin/SCMP2 output pin
			• Interrupt input pin/PWM output pin

FUNCTIONAL DESCRIPTION CENTRAL PROCESSING UNIT (CPU)

The M37516F8HP uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.

The CPU mode register is allocated at address 003B16.

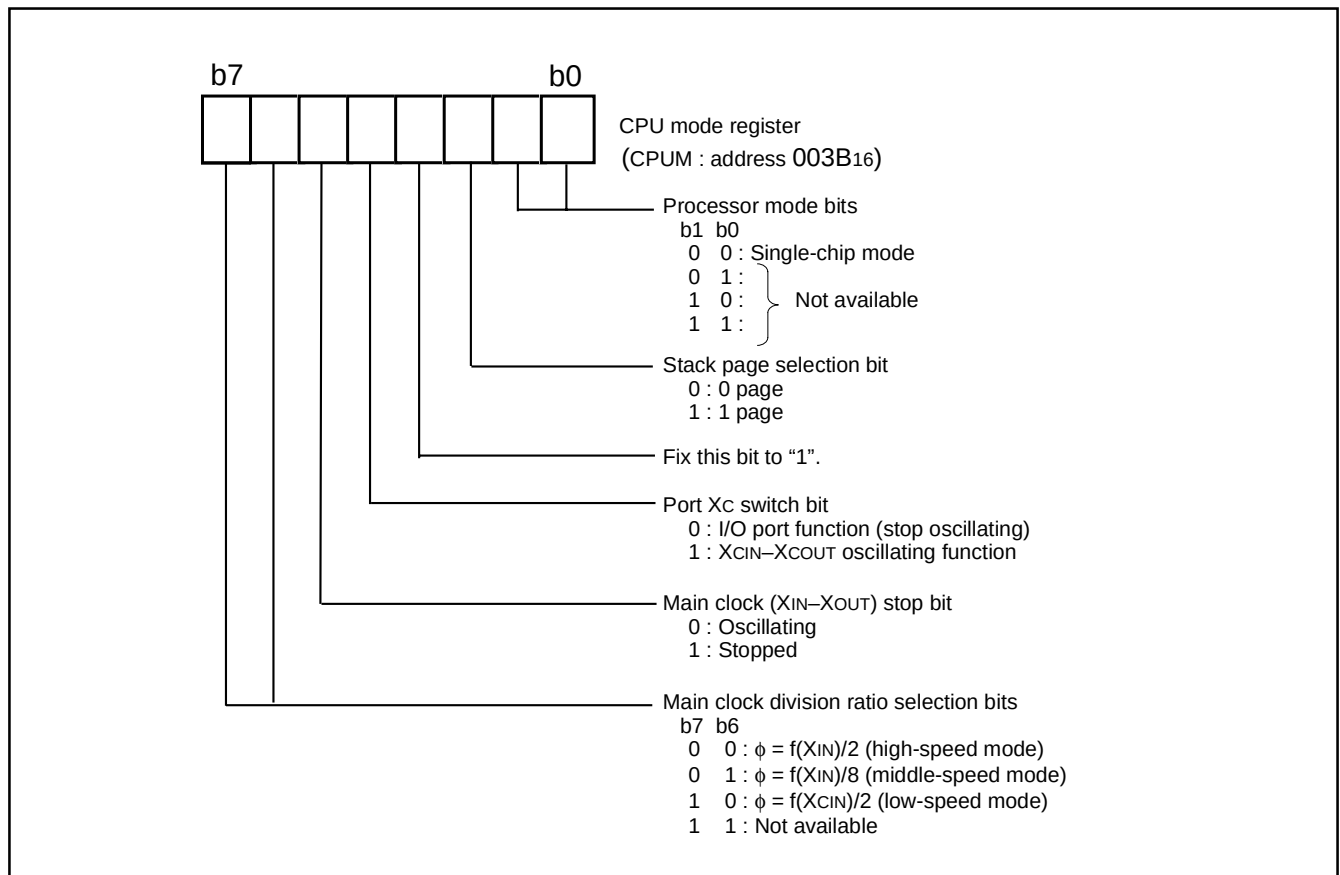


Fig. 3 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

Flash Memory

The first 128 bytes and the last 2 bytes of flash memory are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

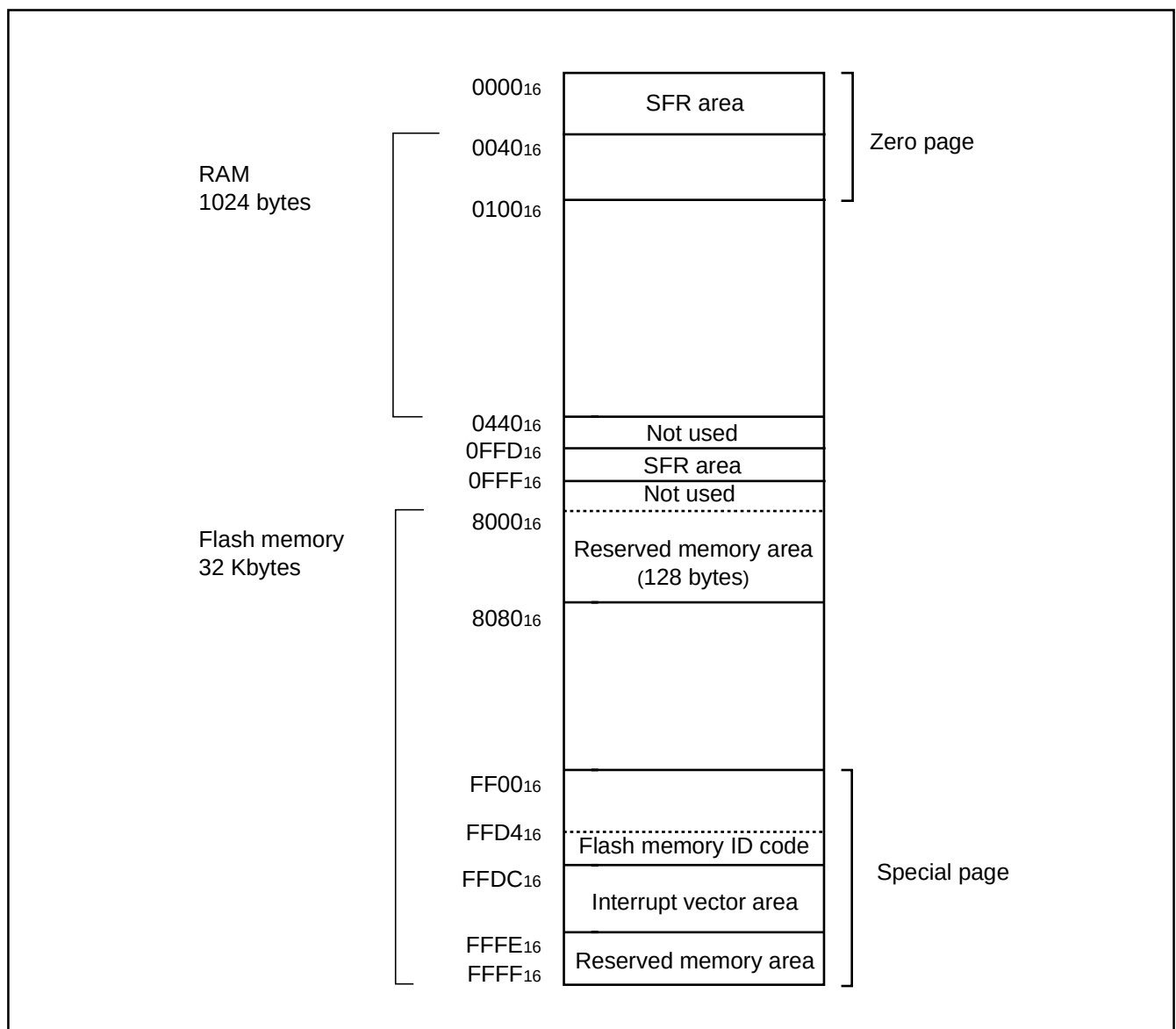


Fig. 4 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Prescaler 12 (PRE12)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 1 (T1)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 2 (T2)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer XY mode register (TM)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Prescaler X (PREX)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer X (TX)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Prescaler Y (PREY)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer Y (TY)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer count source selection register (TCSS)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	
000A ₁₆		002A ₁₆	
000B ₁₆		002B ₁₆	I ² C data shift register (S0)
000C ₁₆		002C ₁₆	I ² C address register (S0D)
000D ₁₆		002D ₁₆	I ² C status register (S1)
000E ₁₆		002E ₁₆	I ² C control register (S1D)
000F ₁₆		002F ₁₆	I ² C clock control register (S2)
0010 ₁₆		0030 ₁₆	I ² C start/stop condition control register (S2D)
0011 ₁₆		0031 ₁₆	Reserved *
0012 ₁₆	Reserved *	0032 ₁₆	
0013 ₁₆	Reserved *	0033 ₁₆	
0014 ₁₆	Reserved *	0034 ₁₆	A-D control register (ADCON)
0015 ₁₆	Serial I/O2 control register 1 (SIO2CON1)	0035 ₁₆	A-D conversion low-order register (ADL)
0016 ₁₆	Serial I/O2 control register 2 (SIO2CON2)	0036 ₁₆	A-D conversion high-order register (ADH)
0017 ₁₆	Serial I/O2 register (SIO2)	0037 ₁₆	Reserved *
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	MISRG
0019 ₁₆	Serial I/O1 status register (SIOSTS)	0039 ₁₆	Watchdog timer control register (WDTCN)
001A ₁₆	Serial I/O1 control register (SIOCON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	PWM control register (PWMCON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	PWM prescaler (PREPWM)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	PWM register (PWM)	003F ₁₆	Interrupt control register 2 (ICON2)
		0FFD ₁₆	Reserved *
		0FFE ₁₆	Flash memory control register (FCON)
		0FFF ₁₆	Reserved *

* Reserved : Do not write any data to the reserved area.

Fig. 5 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

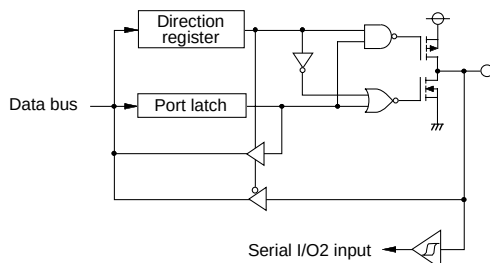
When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

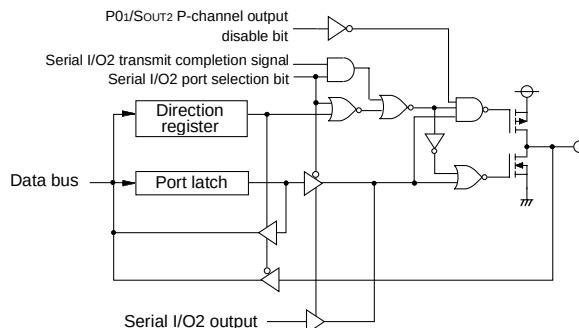
Table 2 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
P04–P07						(5)
P10–P17	Port P1					
P20/XCOUT P21/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
P22/SDA1 P23/SCL1				I ² C-BUS interface func- tion I/O	I ² C control register	(8) (9)
P24/SDA2/RxD P25/SCL2/TxD			CMOS compatible input level CMOS/SMBUS input level (when selecting I ² C-BUS interface function) N-channel open-drain output	I ² C-BUS interface func- tion I/O	I ² C control register Serial I/O1 control register	(10) (11)
P26/SCLK			CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register	(12)
P27/CNTR0/ SRDY1				Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(13)
P30/AN0– P37/AN7	Port P3			A-D conversion input	A-D control register	(14)
P40/CNTR1	Port P4			Timer Y function I/O	Timer XY mode register	(15)
P41/INT0 P42/INT1				External interrupt input	Interrupt edge selection register	(16)
P43/INT2/SCMP2				External interrupt input SCMP2 output	Interrupt edge selection register Serial I/O2 control register	(17)
P44/INT3/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(18)
P45–P47						(5)

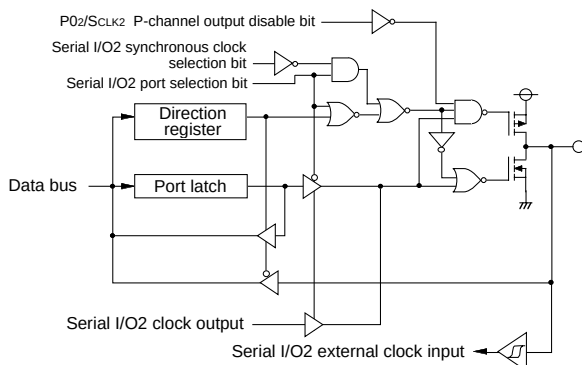
(1) Port P00



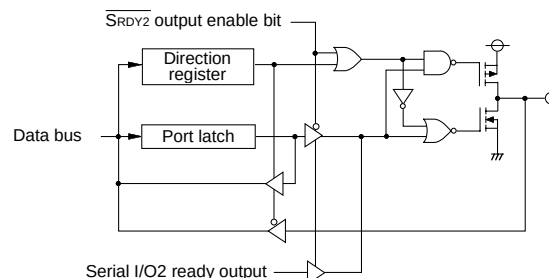
(2) Port P01



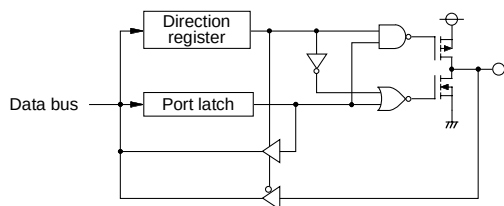
(3) Port P02



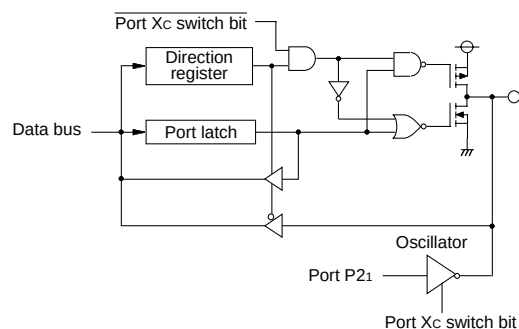
(4) Port P03



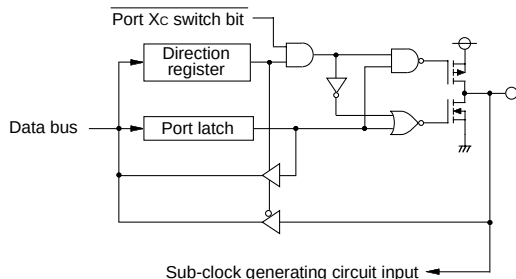
(5) Ports P04–P07, P1, P45–P47



(6) Port P20



(7) Port P21



(8) Port P22

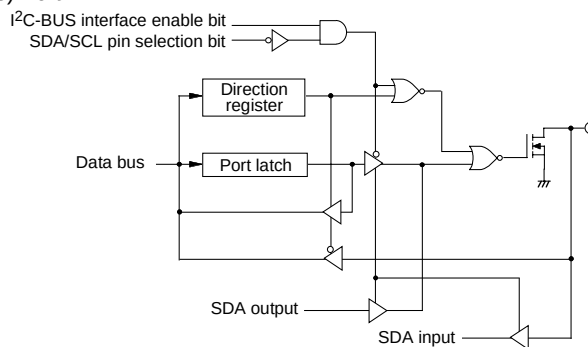
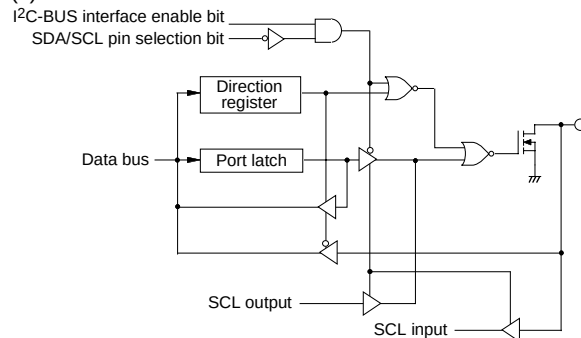
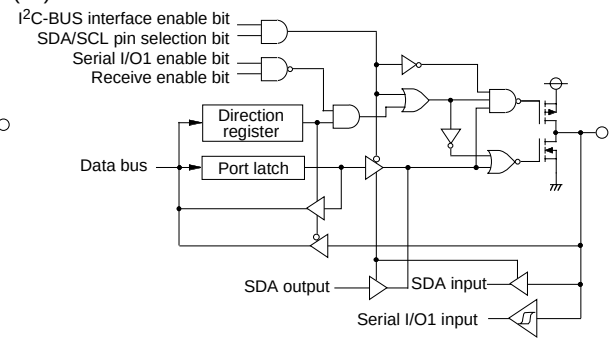


Fig. 6 Port block diagram (1)

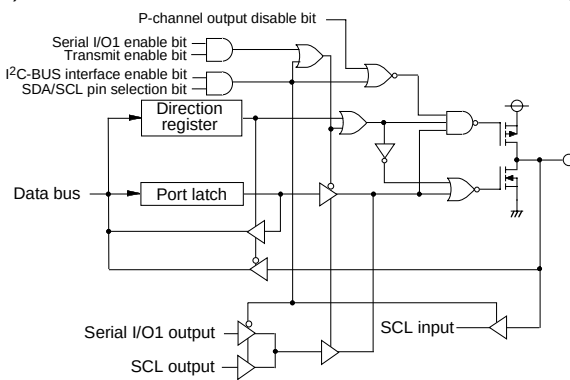
(9) Port P23



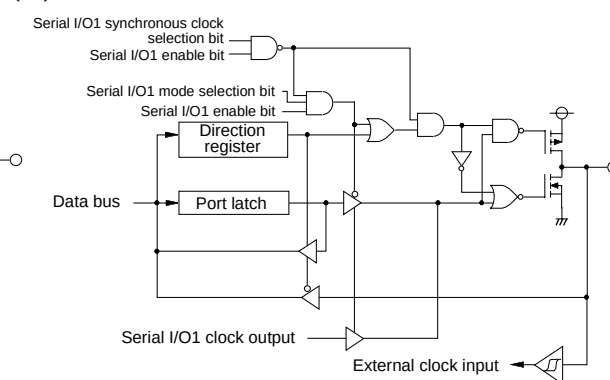
(10) Port P24



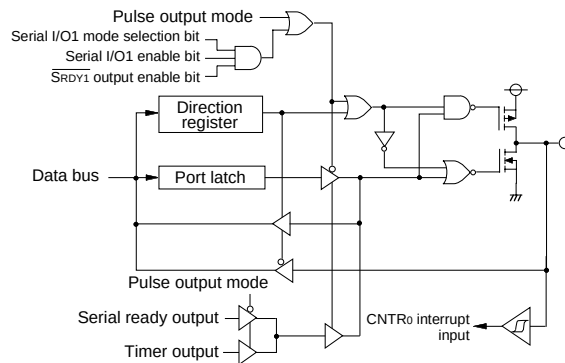
(11) Port P25



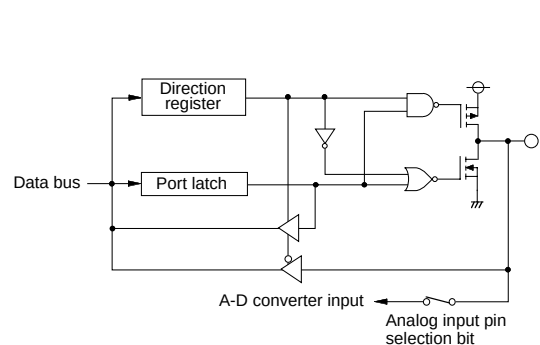
(12) Port P26



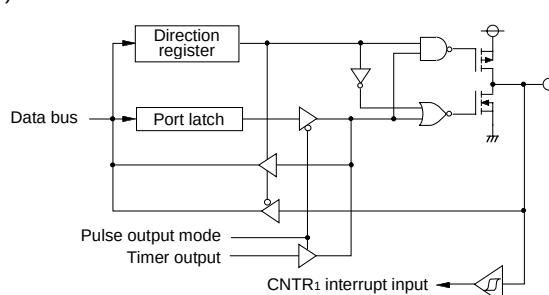
(13) Port P27



(14) Ports P30-P37



(15) Port P40



(16) Ports P41, P42

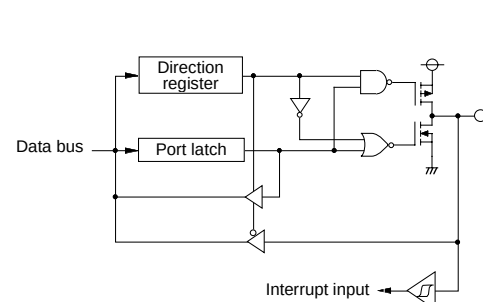


Fig. 7 Port block diagram (2)

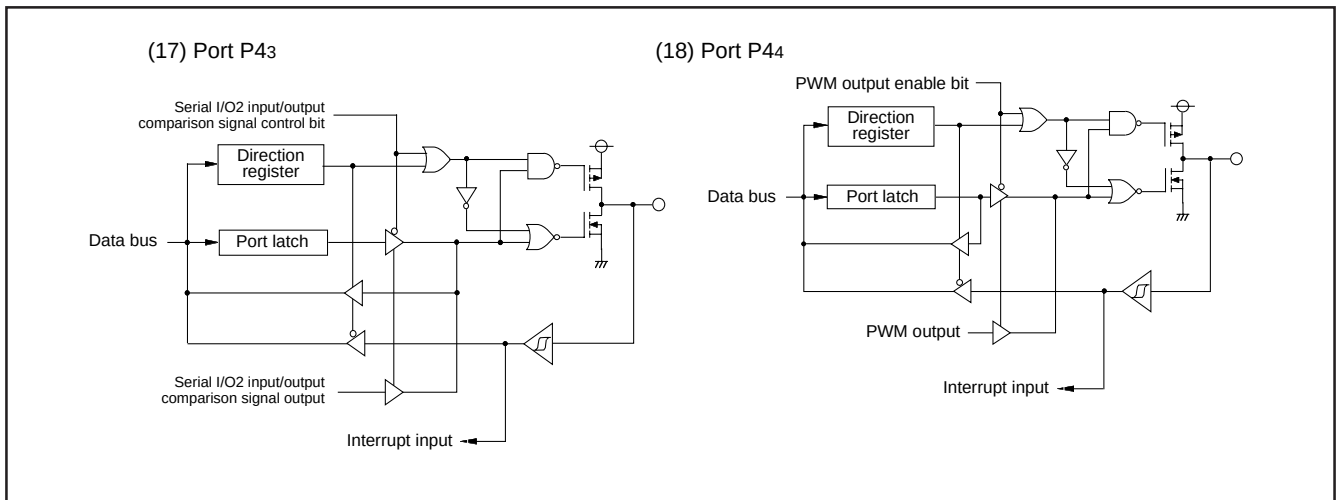
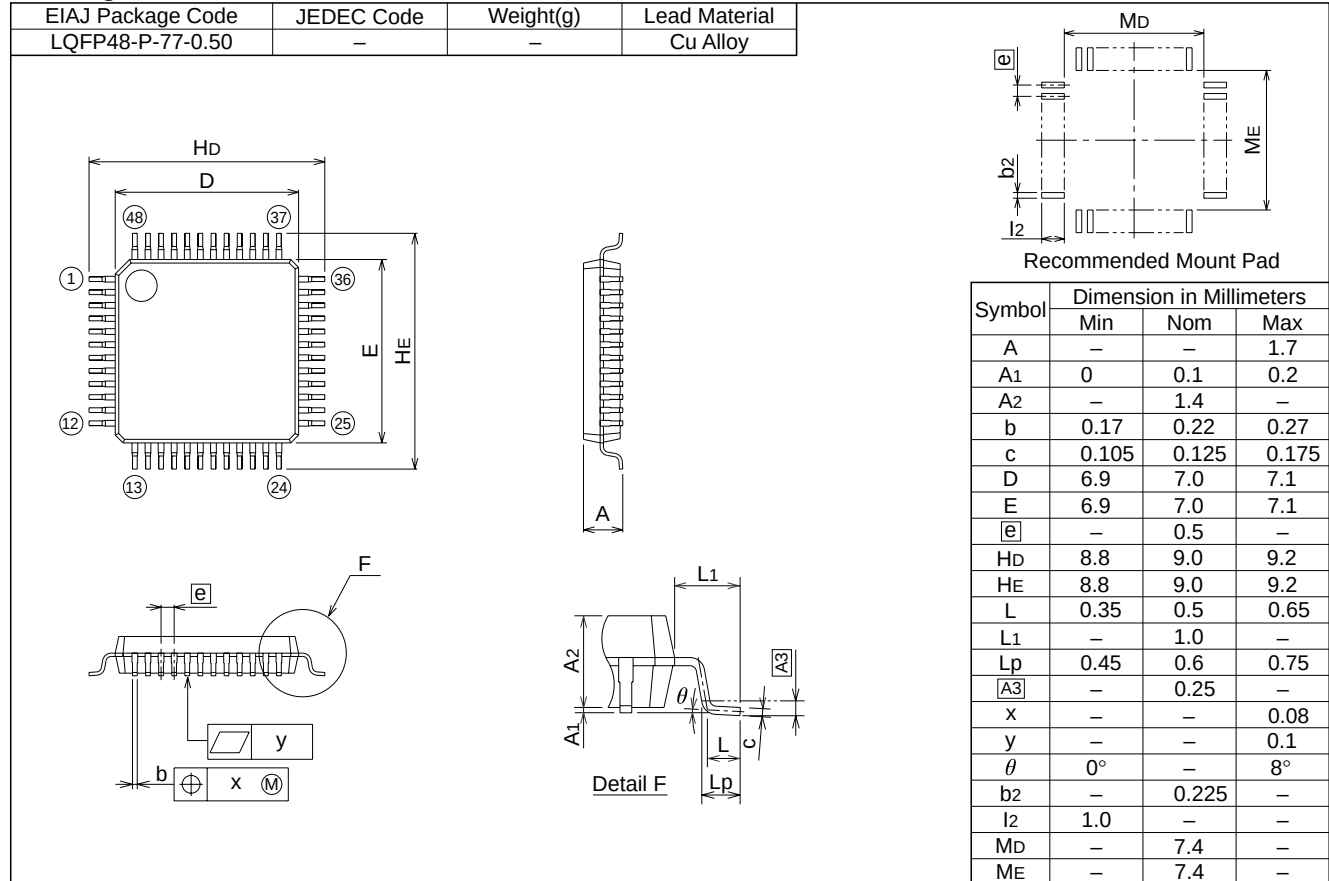


Fig. 8 Port block diagram (3)

PACKAGE OUTLINE

48P6Q-A

Plastic 48pin 7X7mm body LQFP



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REVISION HISTORY	M37516F8HP DATA SHEET
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Rev. No.	Revision Description	Rev. date
0.1	First Edition	2/3/00

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