Designing Power Supplies with

TinySwitch®-III

Seminar Agenda

- **Introduction**
  - Power Integrations
- **Introducing *TinySwitch-III***
  - Features and Operation
  - Performance
  - Designing with *TinySwitch-III*
  - Hints and Tips
  - Design Examples
  - *PI* Device Quick Design Checklist
- **External Power Supply (EPS)**

  Energy Efficiency Standards

Power Integrations Overview

Company Overview

- Leader in high voltage monolithic power conversion ICs
- > 1.6 billion devices shipped
- Revolutionary products
- Proven quality and delivery performance
- Pioneers in energy efficiency (EcoSmart®)

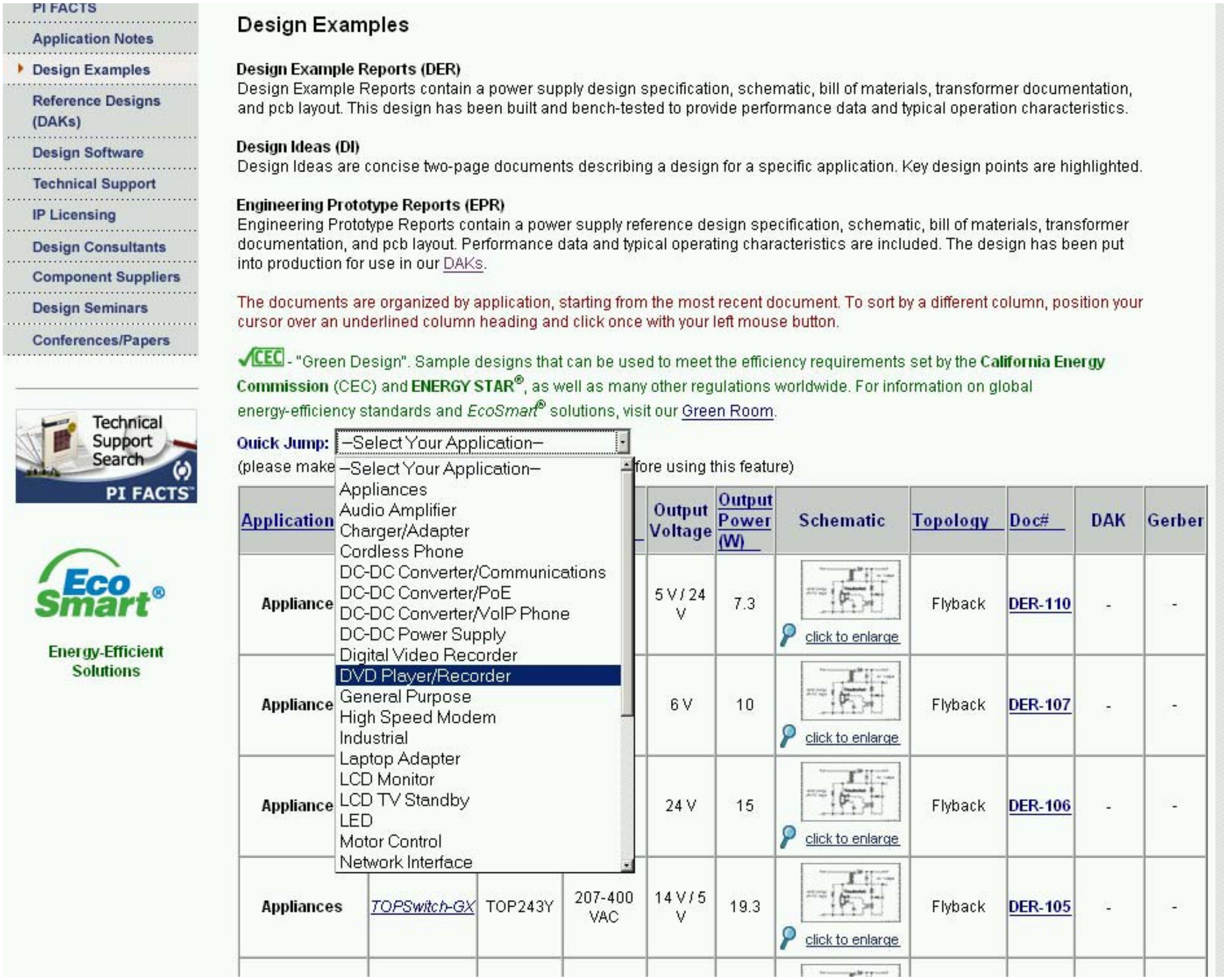
Global Applications Support

- **Fully Equipped Applications Labs**
- **55+ Application Engineers Worldwide**

24-Hour Design Documentation Support

http://www.powerint.com

Design Examples Page Has > 150 Supplies



- PI FACTS
- Application Notes
- Design Examples
- Reference Designs (DAKs)
- Design Software
- Technical Support
- IP Licensing
- Design Consultants
- Component Suppliers
- Design Seminars
- Conferences/Papers

Technical Support Search
PI FACTS

EcoSmart®
Energy-Efficient Solutions

Design Examples

Design Example Reports (DER)
Design Example Reports contain a power supply design specification, schematic, bill of materials, transformer documentation, and pcb layout. This design has been built and bench-tested to provide performance data and typical operation characteristics.

Design Ideas (DI)
Design Ideas are concise two-page documents describing a design for a specific application. Key design points are highlighted.

Engineering Prototype Reports (EPR)
Engineering Prototype Reports contain a power supply reference design specification, schematic, bill of materials, transformer documentation, and pcb layout. Performance data and typical operating characteristics are included. The design has been put into production for use in our DAKs.

The documents are organized by application, starting from the most recent document. To sort by a different column, position your cursor over an underlined column heading and click once with your left mouse button.

CEC - "Green Design". Sample designs that can be used to meet the efficiency requirements set by the **California Energy Commission** (CEC) and **ENERGY STAR®**, as well as many other regulations worldwide. For information on global energy-efficiency standards and *EcoSmart®* solutions, visit our Green Room.

Quick Jump: –Select Your Application–
(please make ... fore using this feature)

- –Select Your Application–
- Appliances
- Audio Amplifier
- Charger/Adapter
- Cordless Phone
- DC-DC Converter/Communications
- DC-DC Converter/PoE
- DC-DC Converter/VoIP Phone
- DC-DC Power Supply
- Digital Video Recorder
- DVD Player/Recorder
- General Purpose
- High Speed Modem
- Industrial
- Laptop Adapter
- LCD Monitor
- LCD TV Standby
- LED
- Motor Control
- Network Interface

Application				Output Voltage	Output Power (W)	Schematic	Topology	Doc#	DAK	Gerber
Appliance				5 V / 24 V	7.3	click to enlarge	Flyback	DER-110	-	-
Appliance				6 V	10	click to enlarge	Flyback	DER-107	-	-
Appliance				24 V	15	click to enlarge	Flyback	DER-106	-	-
Appliances	*TOPSwitch-GX*	TOP243Y	207-400 VAC	14 V / 5 V	19.3	click to enlarge	Flyback	DER-105	-	-

http://www.powerint.com/appcircuits.htm

> 15 Working Reference Designs Available

Power Integrations - Reference Designs (DAKs) - Microsoft Internet Explorer provided by Power Integrations, Inc.

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Reference Designs

Reference Designs (DAKs) provide the essential materials to get started on your next power supply design. All kits include samples, a fully functional reference board and complete documentation. To purchase a DAK, contact your local sales representative or distributor.

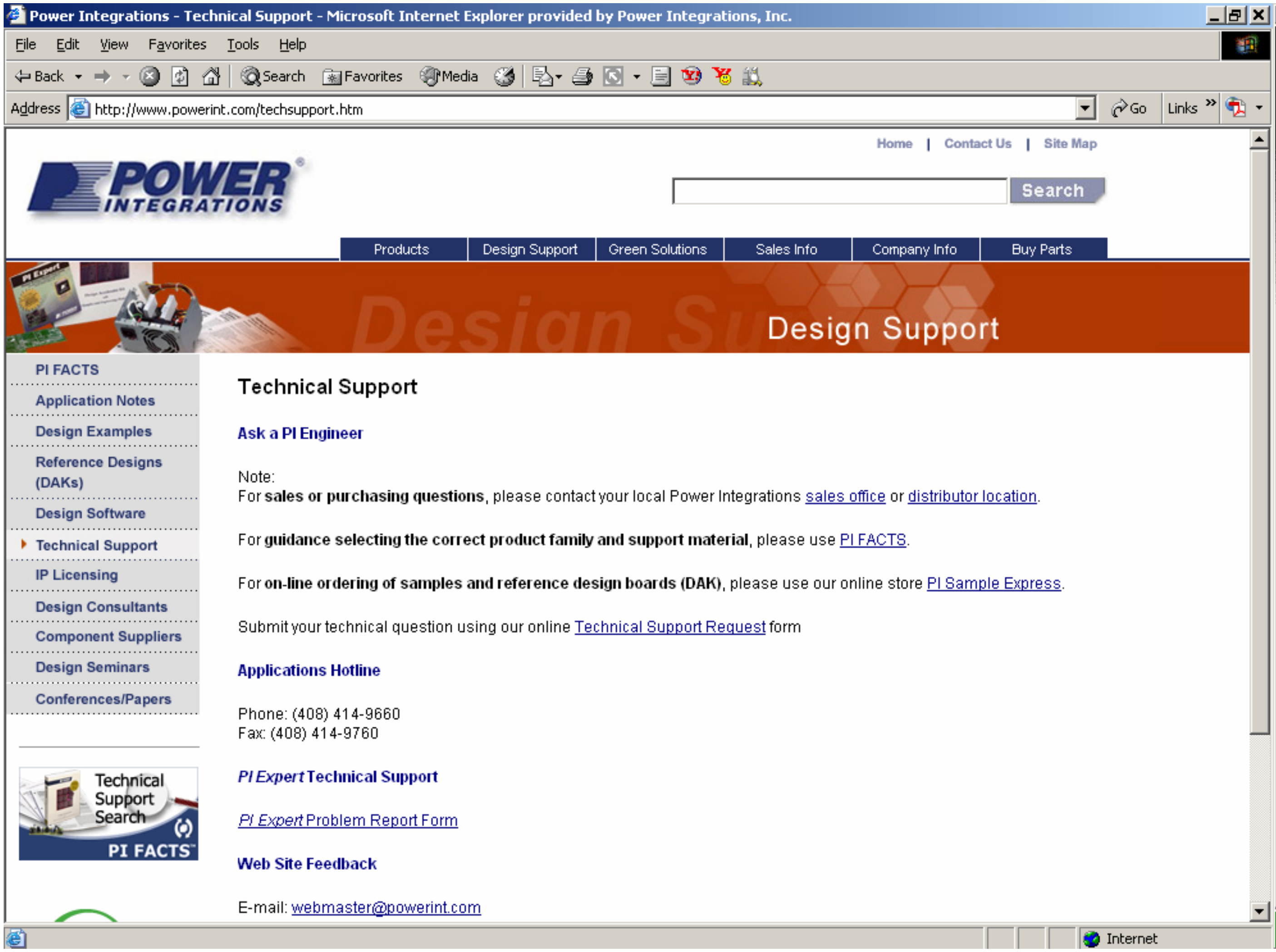
Sample EXPRESS

CEC - "Green Design". Sample designs that can be used to meet the efficiency requirements set by the **California Energy Commission** (CEC) and **ENERGY STAR®**, as well as many other regulations worldwide. For information on global energy-efficiency standards and *EcoSmart®* solutions, visit our Green Room.

DESIGN ACCELERATOR KIT	ENGINEERING PROTOTYPE BOARD					SAMPLES	DOCUMENTATION		
	BOARD NUMBER	PI DEVICE	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT POWER		DATA SHEETS	ENGINEERING REPORT	APPLICATION NOTE
DAK-93 *PeakSwitch* CEC	EP-93	PKS606Y	90-265 VAC	30 V	32 W	PKS604P/Y PKS605P/Y PKS606P/Y	PKS603-606	EPR-93	AN-41
DAK-91 *TinySwitch-III* CEC	EP-91	TNY278P	85-265 VAC	12 V	12 W	TNY279P TNY280P	TNY274-280	EPR-91	-
DAK-89 *LinkSwitch-XT* CEC	EP-89	LNK362P	85-265 VAC	6.2 V	2 W	LNK362P/G LNK363P/G LNK364P/G	LNK362-364	EPR-89	AN-40

http://www.powerint.com/dak.htm

World-Wide Technical Support



http://www.powerint.com/techsupport.htm

Introducing the
TinySwitch®-III
IC Family

The ***TinySwitch®-III*** IC Family

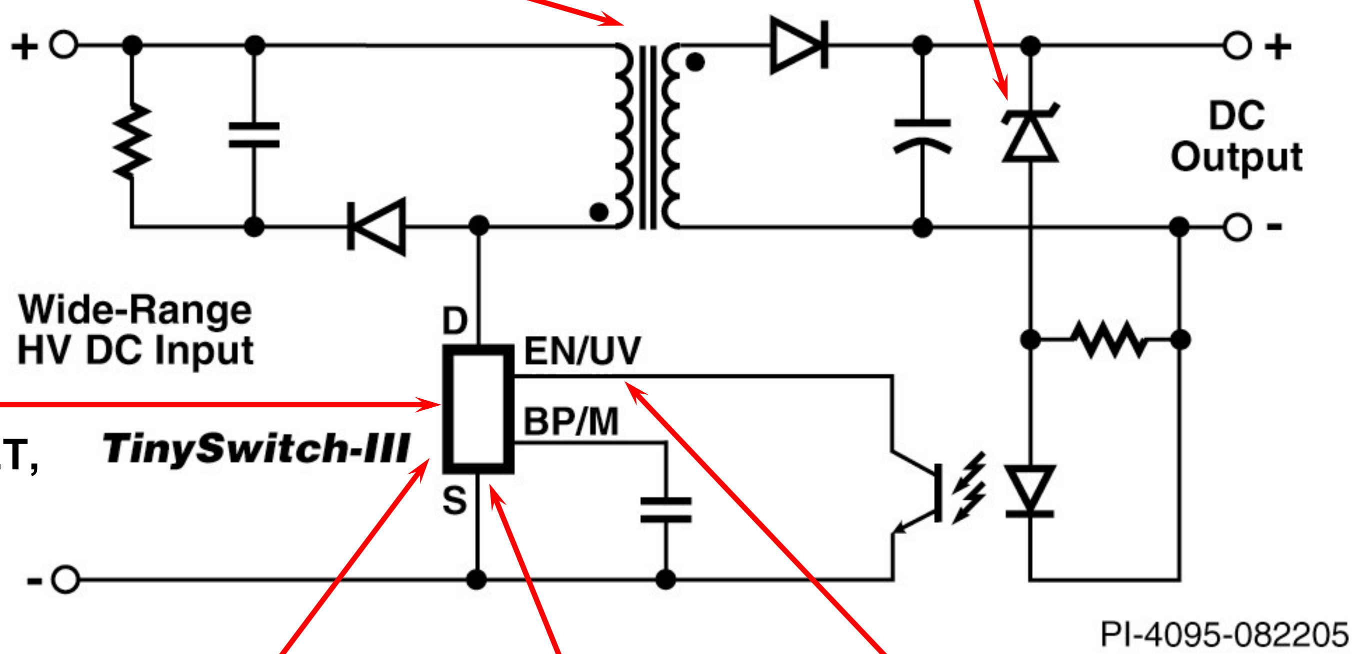
- **A family of highly integrated, off-line switching power conversion ICs**
  - Enables low component count, high reliability power supply solutions
  - New functions and features offer greater flexibility
  - Easily meets all current and proposed energy efficiency standards
  - System-level protection improves reliability
  - Scalable family of devices covers a wide power range up to 36.5 W
  - Optimized pin-out simplifies layout and maximizes heat transfer to PCB

TinySwitch-III Features / System Cost Benefits

132 kHz operation minimizes transformer size

ON/OFF control allows output voltage regulation using a Zener diode reference

Tight I^2f tolerance minimizes MOSFET, transformer and output diode size



Internal, high-voltage, current source eliminates start-up circuitry

Internal current sense circuit eliminates sense resistor

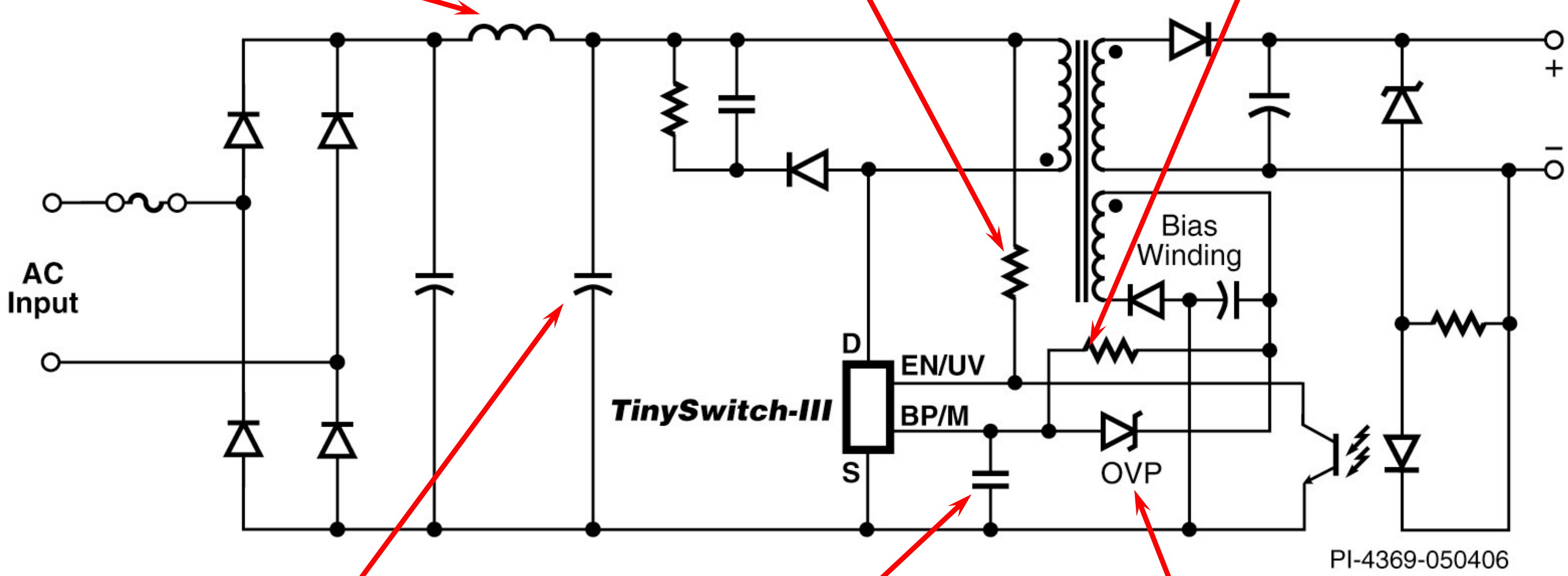
ON/OFF control: no frequency compensation components required

TinySwitch-III Features / System Cost Benefits

Switching frequency jitter enables simple EMI filter

Single resistor UVLO prevents output glitches during power up and shut down

<50 mW no-load consumption with optional bias winding and resistor



On-time extension extends hold-up time to reduce input bulk capacitance

Selectable current limit through BP/M capacitor value for greater flexibility

Latching output overvoltage protection using simple Zener diode eliminates additional opto-coupler

TinySwitch®-III

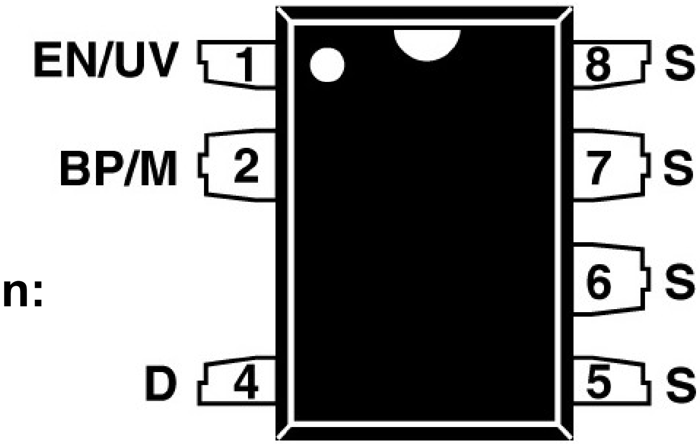
Features and Operation

www.powerint.com

TinySwitch-III Pin Function Descriptions

- **DRAIN (D) Pin:**
  - Power MOSFET drain connection and high-voltage startup
- **BYPASS / Multi-function (BP/M) Pin:**
  - Connection point for bypass capacitor
  - Selects internal current limit level
  - Provides latching shutdown
- **ENABLE / UNDER-VOLTAGE (EN/UV) Pin:**
  - Feedback input for ON/OFF control
  - Senses under-voltage condition
- **SOURCE (S) Pin:**
  - Power MOSFET source connection and controller ground reference

P Package (DIP-8C)
G Package (SMD-8C)

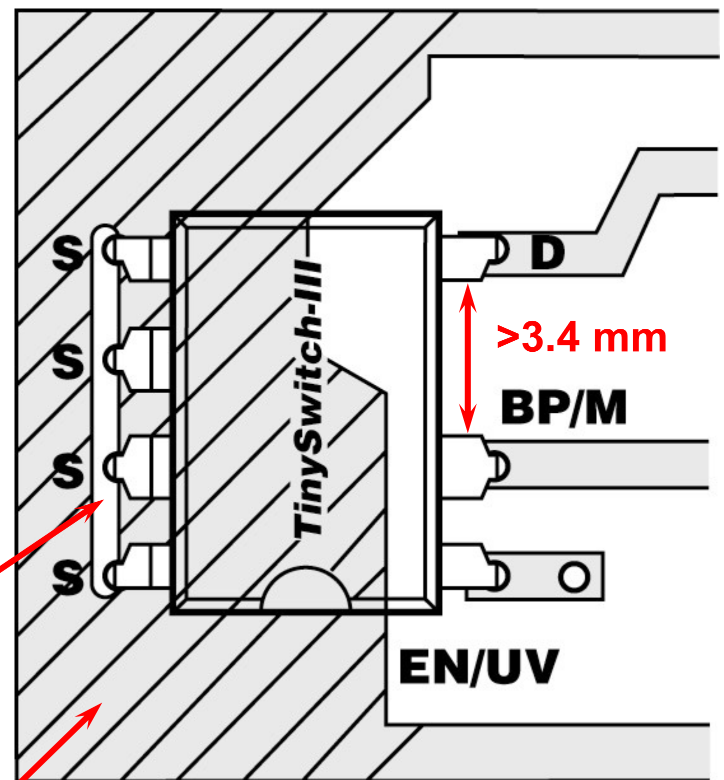


Optimized Package Pin Arrangement Eases Layout For Heatsinking and EMI

- **All SOURCE pins along one side of the package enables use of an additional PCB mounted heatsink**
- **Electrically quiet MOSFET SOURCE is connected to heatsink pins: Lowers EMI generation**

Optional slot for insertion of heatsink

Electrically quiet copper area

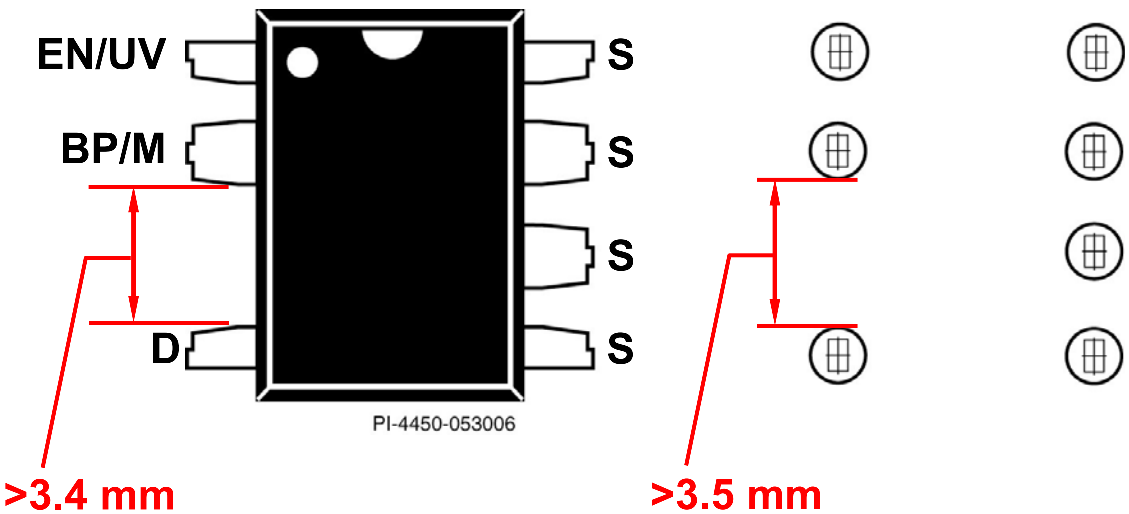


PI-4399-042606

Simplified PCB Layout Improves Heatsinking

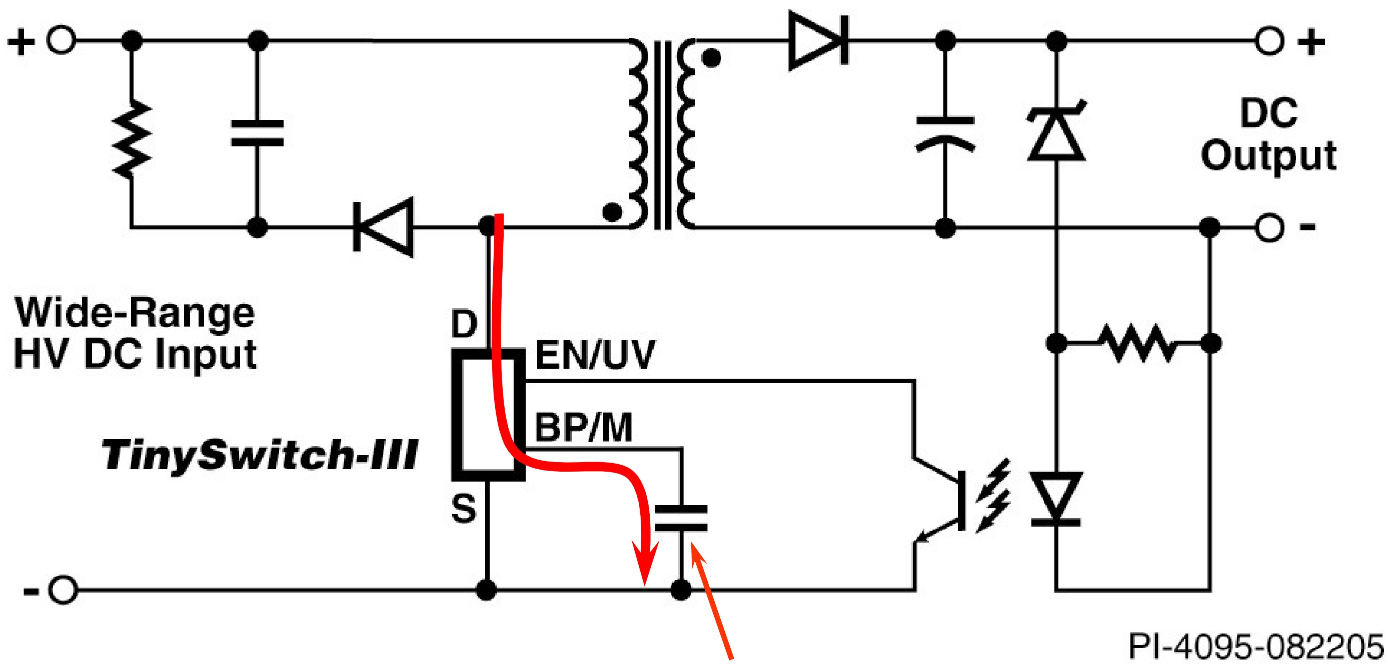
Wide Creepage Distances

- **Extended package and PCB creepage**
  - Industry standard 8 pin package with pin 3 removed
  - Provides adequate high voltage spacing for high humidity and high pollution environments, both at the IC package and on the PCB
  - Meets safety agency functional insulation spacing requirements (3 mm)
    - Eliminates need to short circuit DRAIN pin to any other pin of the IC package



Compare to TO-92 package with < 0.9 mm package creepage

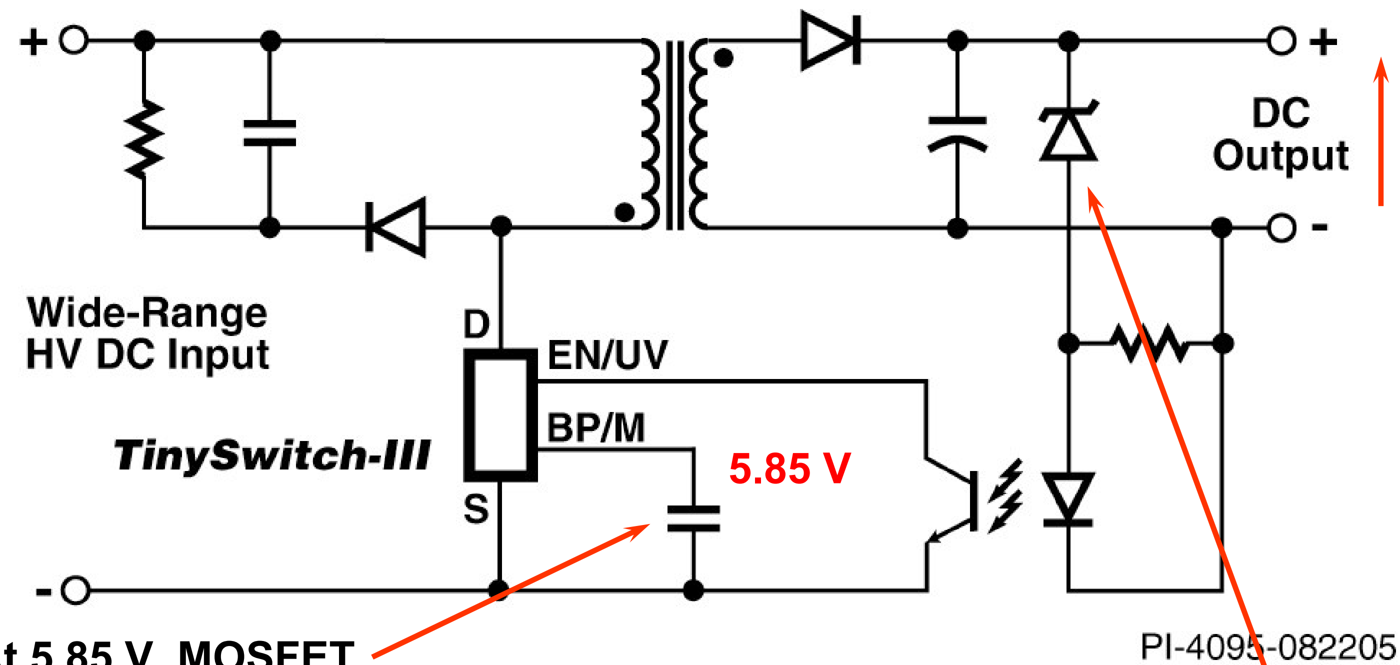
Start-up: Charging BP Pin Capacitor



BP pin capacitor is charged to 5.85 V before MOSFET switching is enabled

- **No external resistor string or start-up circuit required**
- **Value of bypass capacitor selects one of three internal current limits**

Start-up: MOSFET Starts Switching

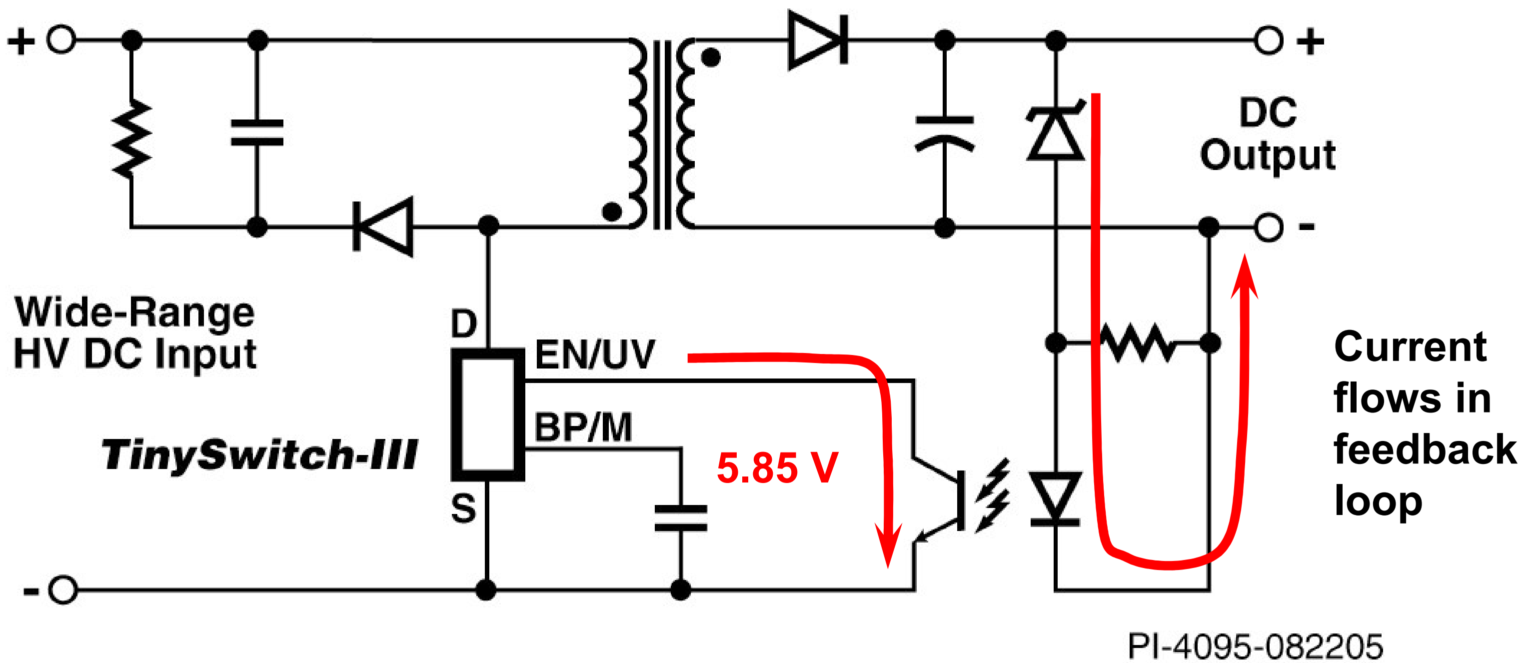


At 5.85 V, MOSFET starts switching

As output voltage rises, no switching cycles are skipped until Zener reference conduction

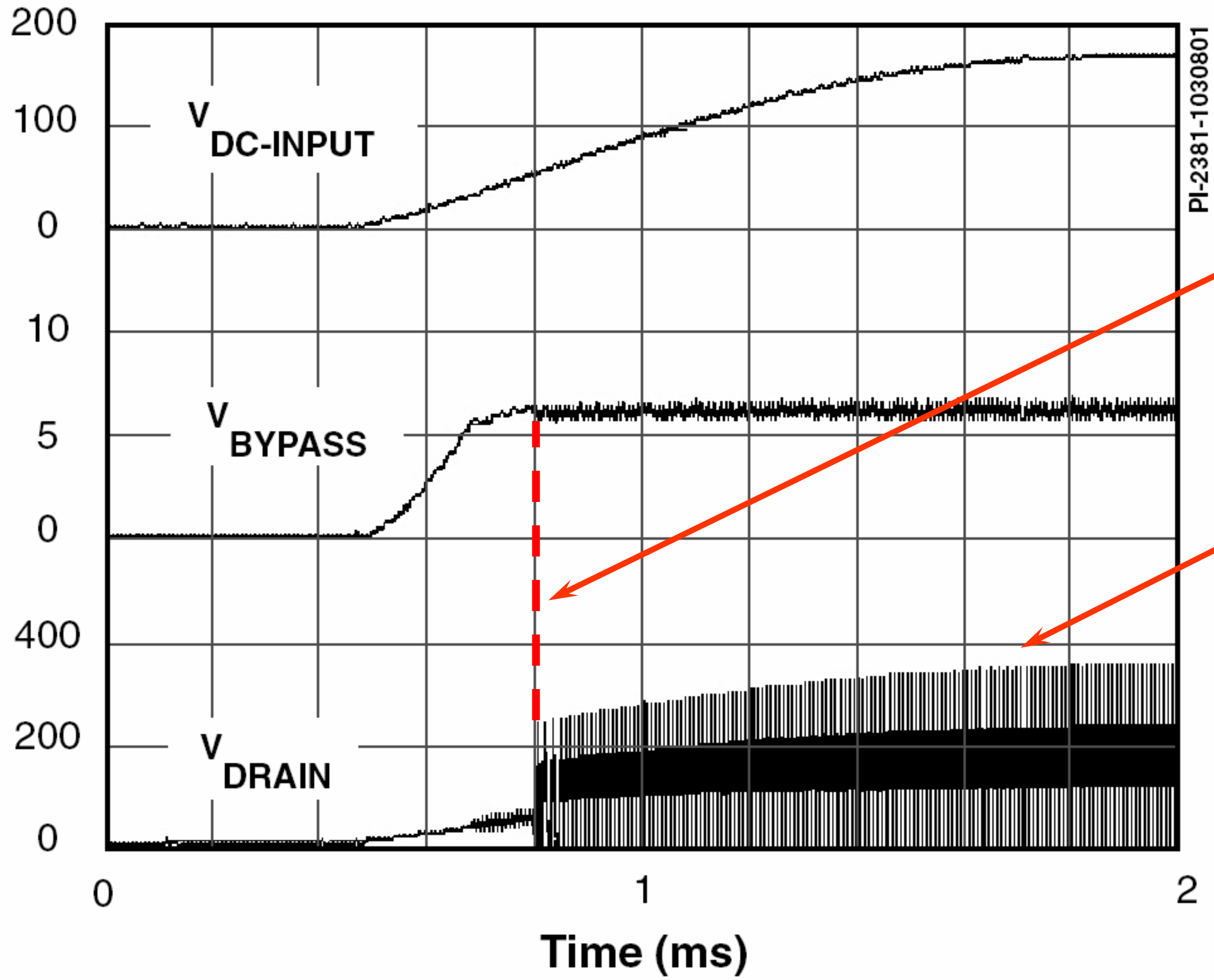
The BP pin capacitor energy powers the IC while MOSFET is on; the internal high-voltage current source recharges the BP pin capacitor while MOSFET is off

Start-up: Output Reaches Regulation



Once output reaches regulation, EN/UV is pulled low, disabling MOSFET switching and regulating the output

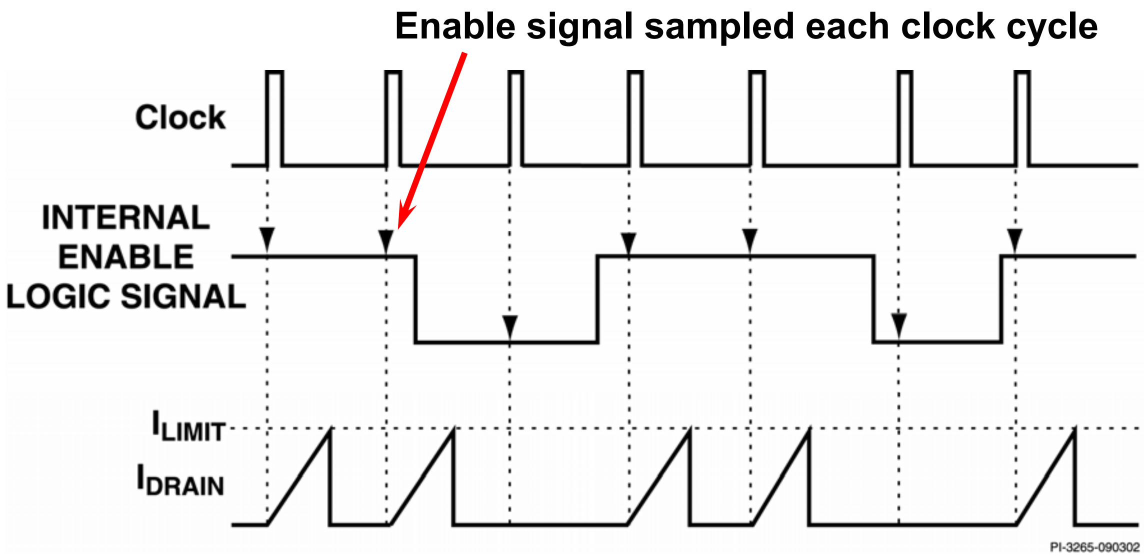
TinySwitch-III Start-up Waveforms



MOSFET switching enabled when BP pin reaches 5.85 V

TinySwitch-III **skipping switching cycles to keep output voltage in regulation**

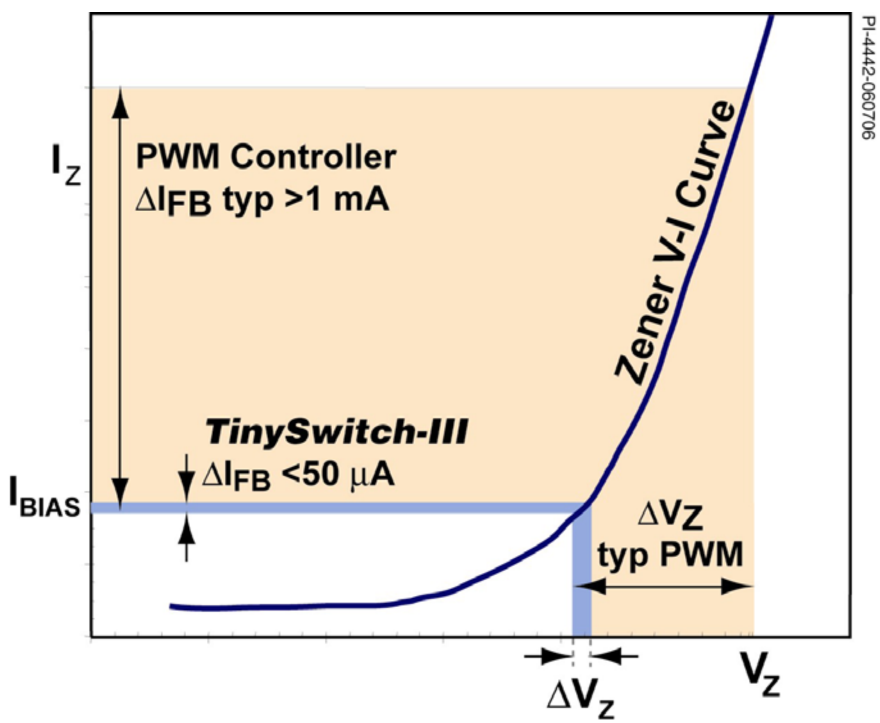
ON/OFF Control Operation and Benefits

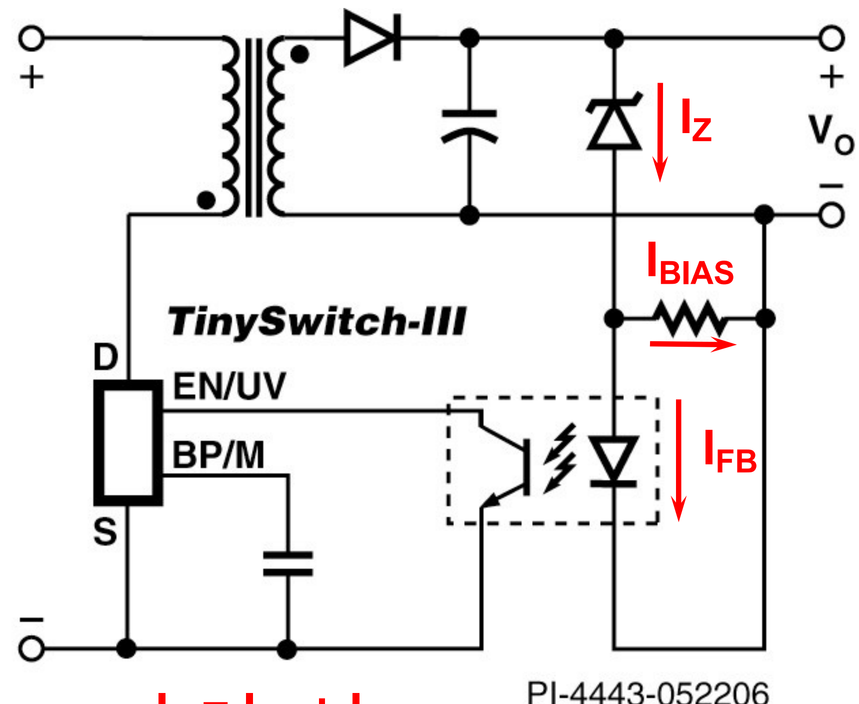


- **MOSFET current ramps to a fixed limit every enabled (ON) switch cycle**
  - Switching cycles are disabled to maintain regulation
- **Effective switching frequency is proportional to load**
  - Efficiency is virtually constant over entire load range, even in standby mode
  - Multi-level MOSFET current limit practically eliminates audible noise
- **No loop compensation components required**

ON/OFF Control Benefit: Output Regulation

- **Overall ± 7% V_o tolerance with (± 2%) Zener feedback (saves cost)**
  – Feedback current (**I_{FB}**) virtually independent of changes in Zener bias point
    - Zener voltage change (ΔV_Z) is very small with ON/OFF control
- **Typical PWM controllers have >1 mA ΔI_{BIAS}, so ΔV_Z affects accuracy**

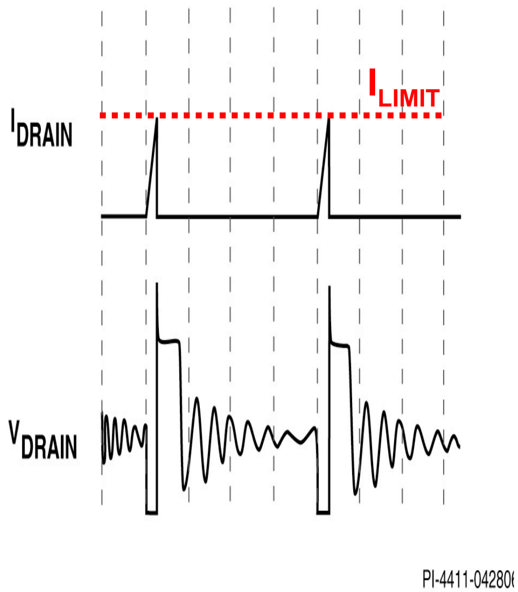




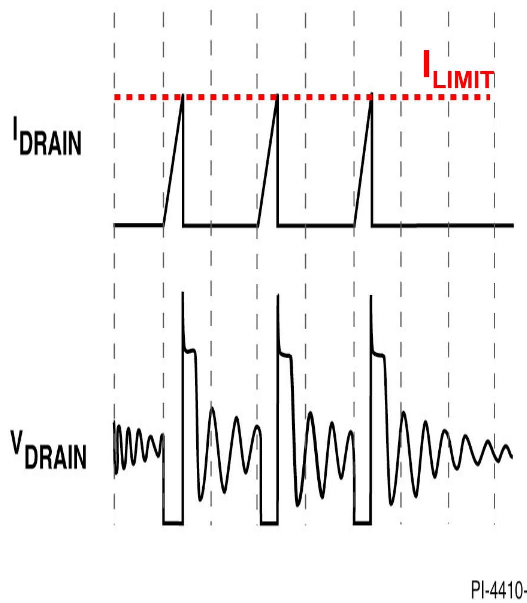
$I_Z = I_{FB} + I_{BIAS}$

Current Limit State Machine Operation

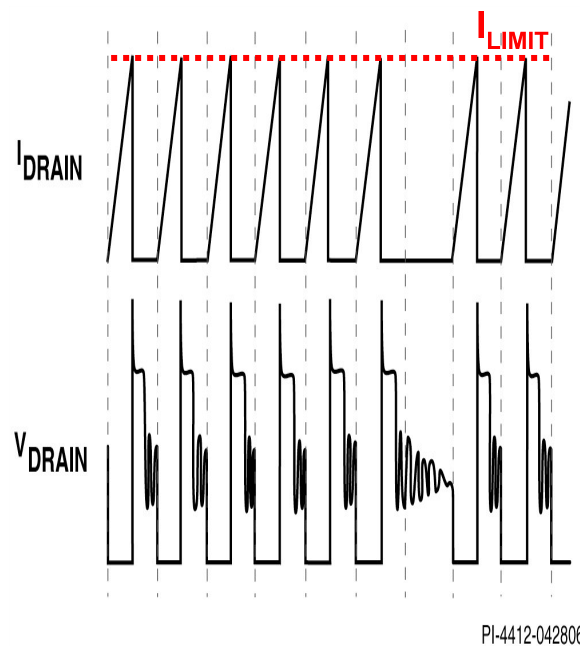
Light Load
I_{LIMIT} = 40%



Mid Load
I_{LIMIT} = 70%



Full Load
I_{LIMIT} = 100%

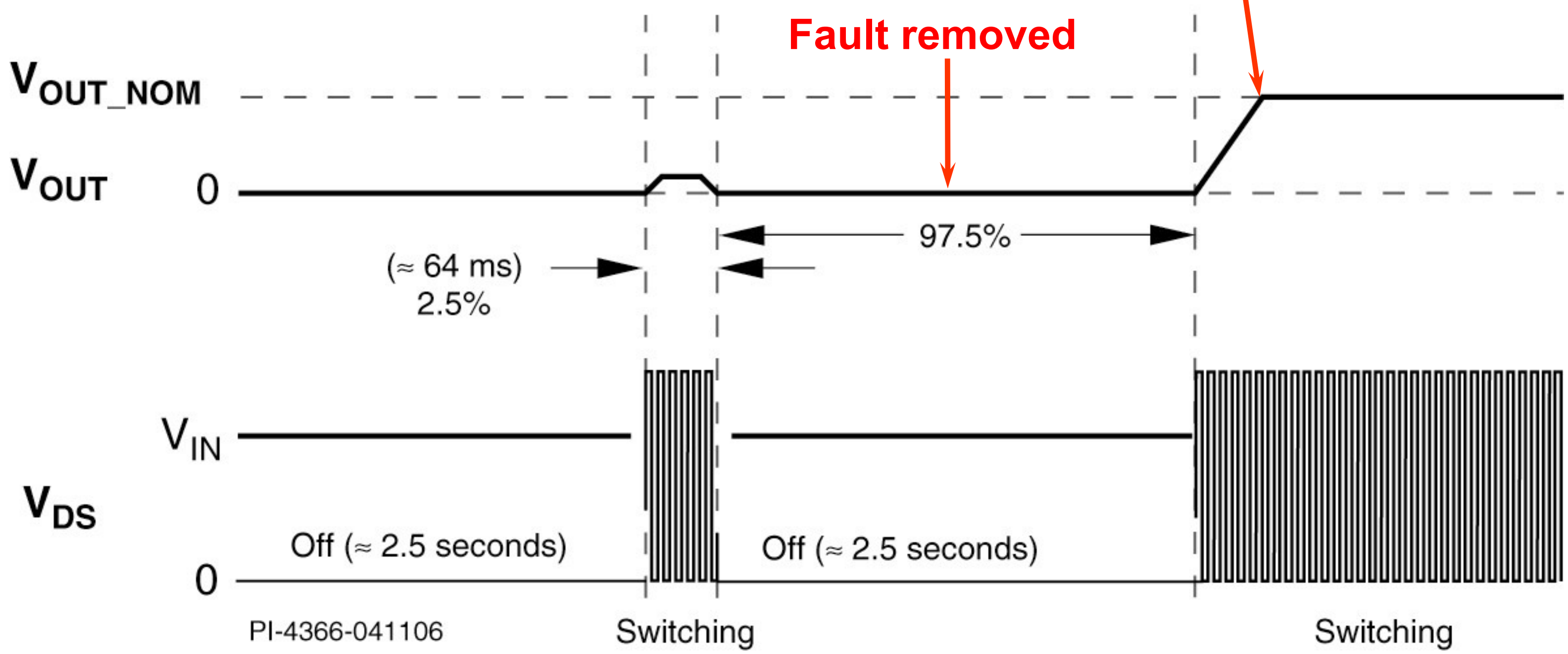


- **The controller sets the MOSFET current limit (I_{LIMIT}) to keep the effective switching frequency above the audible range**

TinySwitch-III Auto-restart Waveforms

When switching cycles are not skipped (<115 µA is drawn from the EN/UV pin) for >64 ms, auto-restart initiates, and MOSFET switching is disabled for ≈ 2.5 s, then re-enabled for 64 ms

Auto-restart ends when >115 µA is drawn from the EN/UV pin while MOSFET switching is enabled (cycle skipping is occurring)



- **Auto-restart limits average output power to < 3% of maximum power**

Selectable MOSFET Current Limit Provides Design Flexibility

DEVICE	CURRENT LIMIT (mA)		
	BP/M cap 1 µF $I_{LIMITred}$	BP/M cap 0.1 µF I_{LIMIT}	BP/M cap 10 µF $I_{LIMITinc}$
TNY274*	210	250	210
TNY275	250	275	350
TNY276	275	350	450
TNY277	350	450	550
TNY278	450	550	650
TNY279	550	650	750
TNY280	650	750	850

PI-4418-050406

* 250 mA is max current limit of the TNY274
All BP/M capacitor values ≥1 µF select $I_{LIMITred}$

- $I_{LIMITred}$ equals the standard I_{LIMIT} of the next smaller device
- $I_{LIMITinc}$ equals the standard I_{LIMIT} of the next larger device
- Optimum device and current limit by simply changing the value of the BP/M pin capacitor
  - $I_{LIMITinc}$ = highest power solution
  - $I_{LIMITred}$ = highest efficiency
- Enables same supply to be used in applications with different ambient temperatures

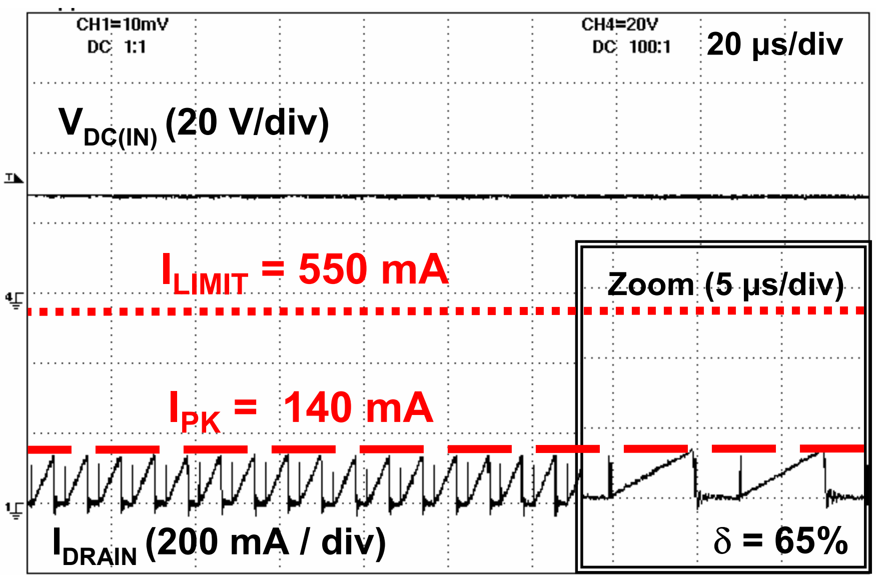
Selectable MOSFET Current Limit Provides Design Flexibility

- **3 current limit levels available for each device (except TNY274)**
  - Current limit levels selected by BP/M pin capacitor value
- **Standard current limit (I_{LIMIT})**
  - Normal choice for sealed enclosure (adapter) applications
- **Higher current limit ($I_{LIMITinc}$)**
  - Extends maximum continuous power in open frame applications
  - Boosts peak power capability in all applications
- **Lower current limit ($I_{LIMITred}$)**
  - Lowers RMS currents and R_{DS_ON} based I^2R losses
    - Lowers the operating temperature of the IC and the supply
    - Improves the active-mode efficiency of the supply
- **Different devices can be used in the same design**
  - A sealed adapter uses one device larger than open frame but with $I_{LIMITred}$

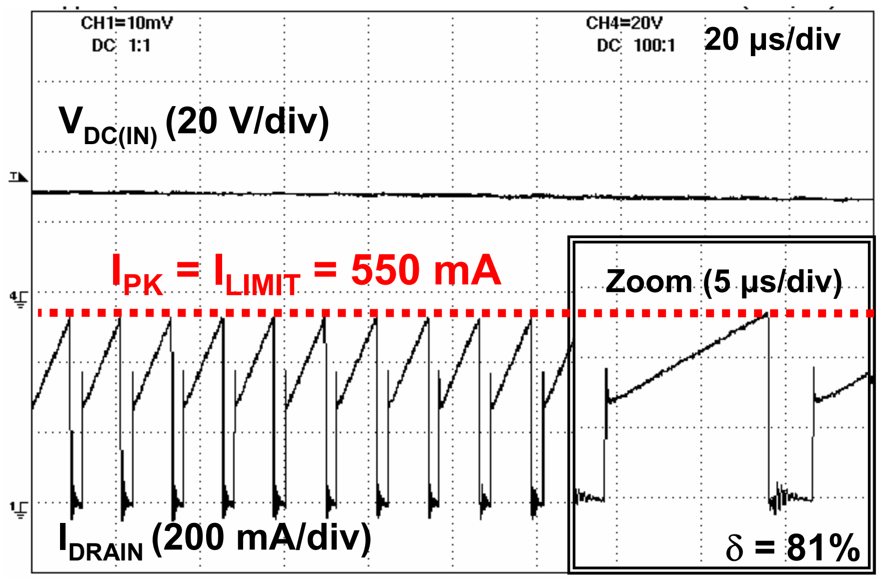
MOSFET On-Time Extension Operation

- **Controller extends ON-time when I_{LIMIT} is not reached by DC_{MAX}**
  - Enables current limit to be reached independent of DC bus voltage
- **Maximizes power capability at very low DC bus voltages**
  - Improves power delivery during line sags, brown-outs and shutdown

Without On-Time Extension

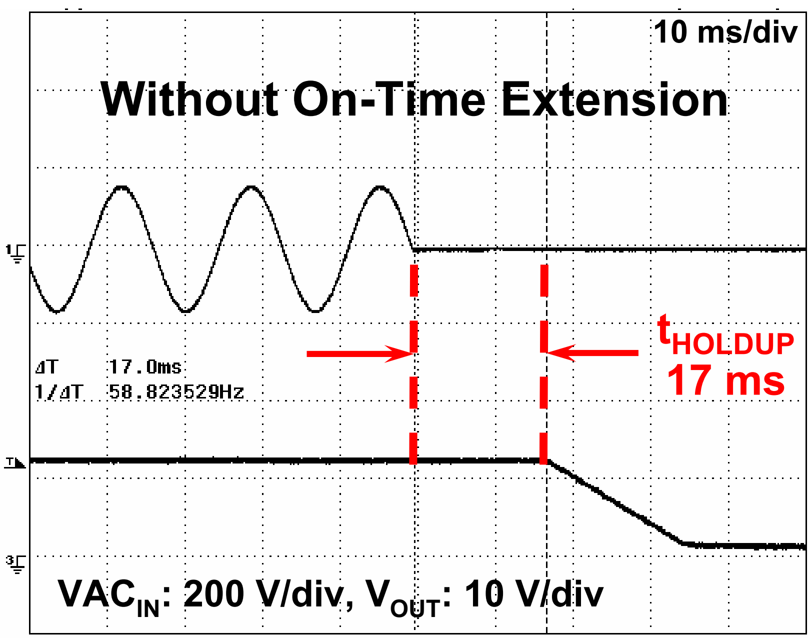


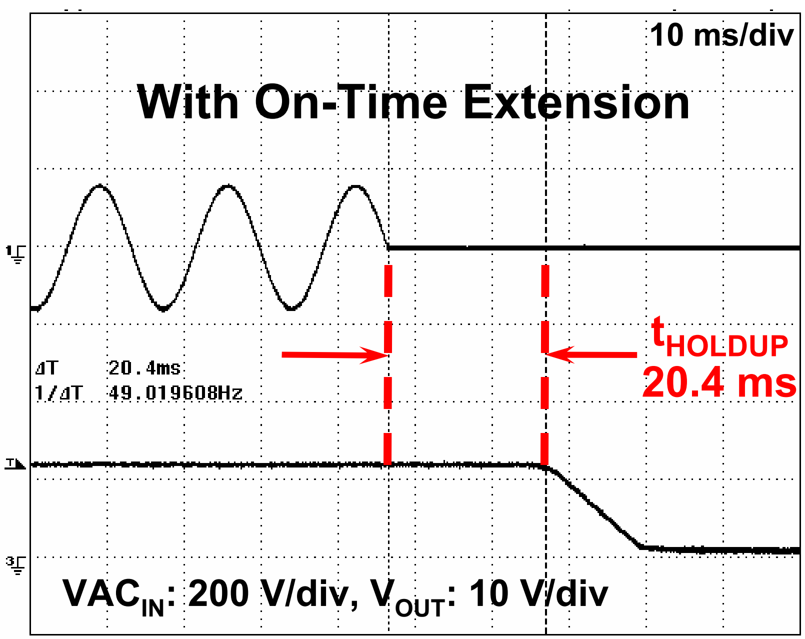
With On-Time Extension



MOSFET On-Time Extension Benefit: Longer Holdup Time

- ON-time extension increases typical output holdup time
- All the energy stored in the bulk capacitance is delivered to output
- May enable smaller values of bulk capacitance to be used

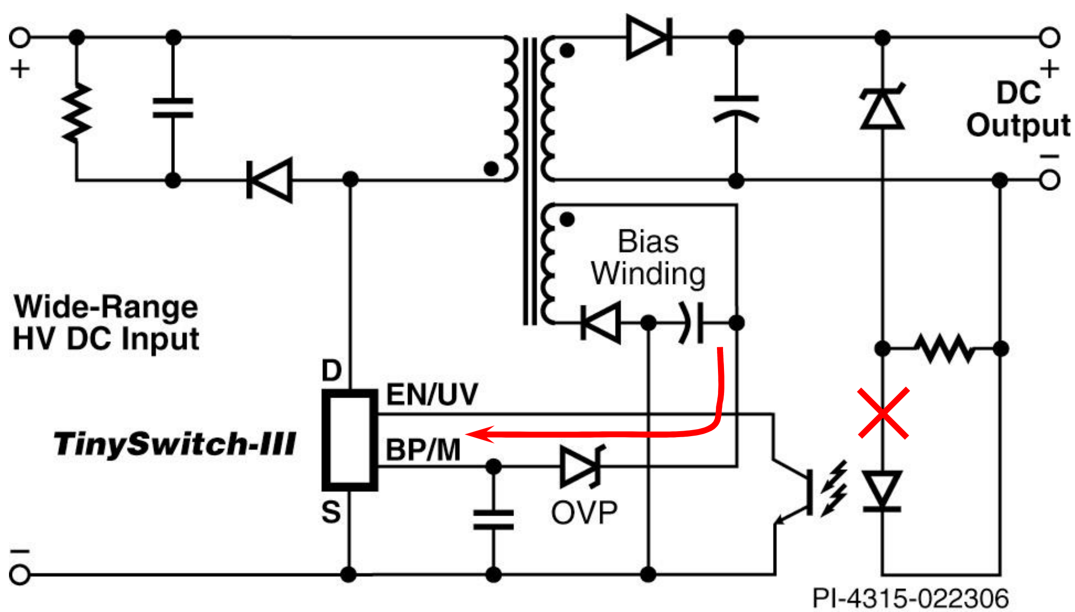




Latching Shutdown for Output Overvoltage Protection (OVP)

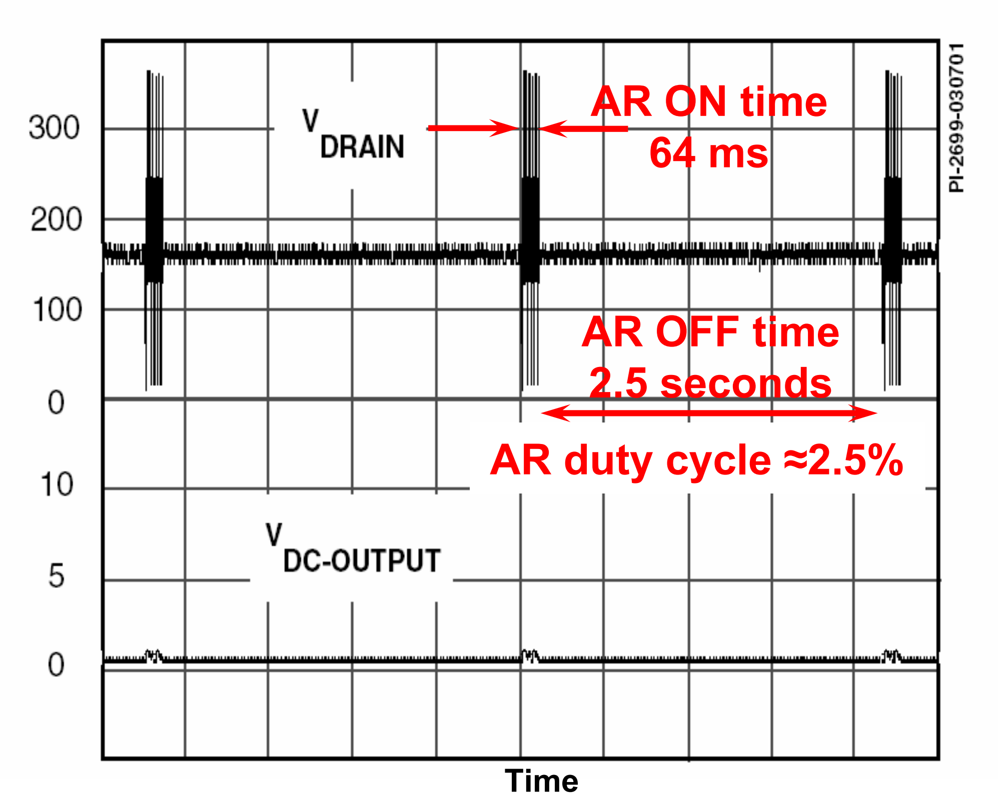
- **Latching shutdown triggers when BP/M pin current >6 mA for >30 μs**
  - 30 μs filter prevents false triggering due to noise or line transients
- **Allows simple, low cost, primary side design**
  - Zener diode connected to bias supply senses output overvoltage
    - Protects against open loop due to component failure or open pin faults

- **Removal of AC input allows input capacitor to discharge**
  - Latch resets when BP/M pin voltage falls below 4.8 V



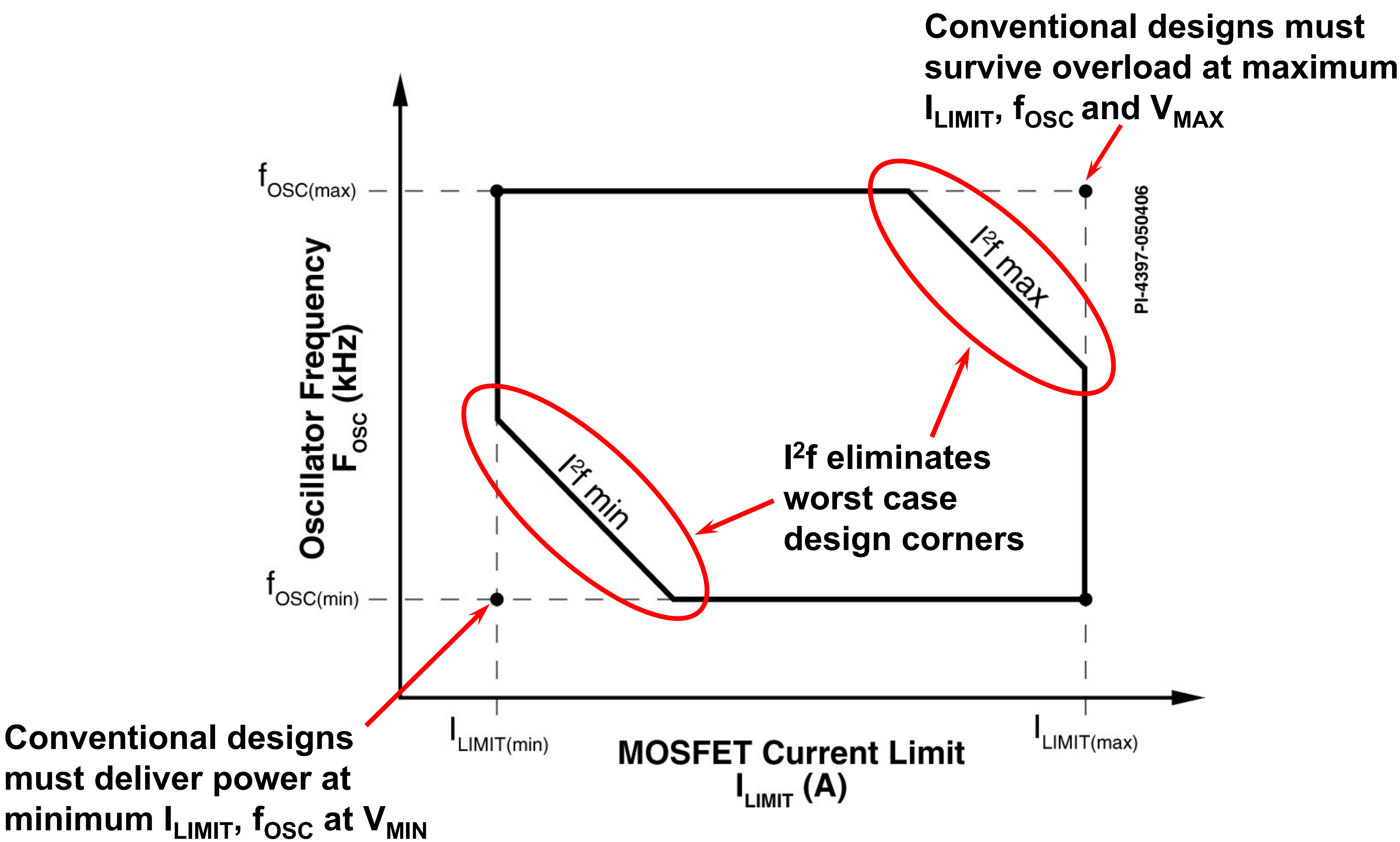
Auto-Restart Function

- **Delivers < 3% of maximum output power during a fault condition**
  - Lowers dissipation in primary clamp, MOSFET, transformer, and output diode
  - Reduces size and cost of the output-clamp Zener diode, if one is used for output overvoltage protection



Typical waveform during auto-restart (AR)

I^2f Parameter Simplifies Design



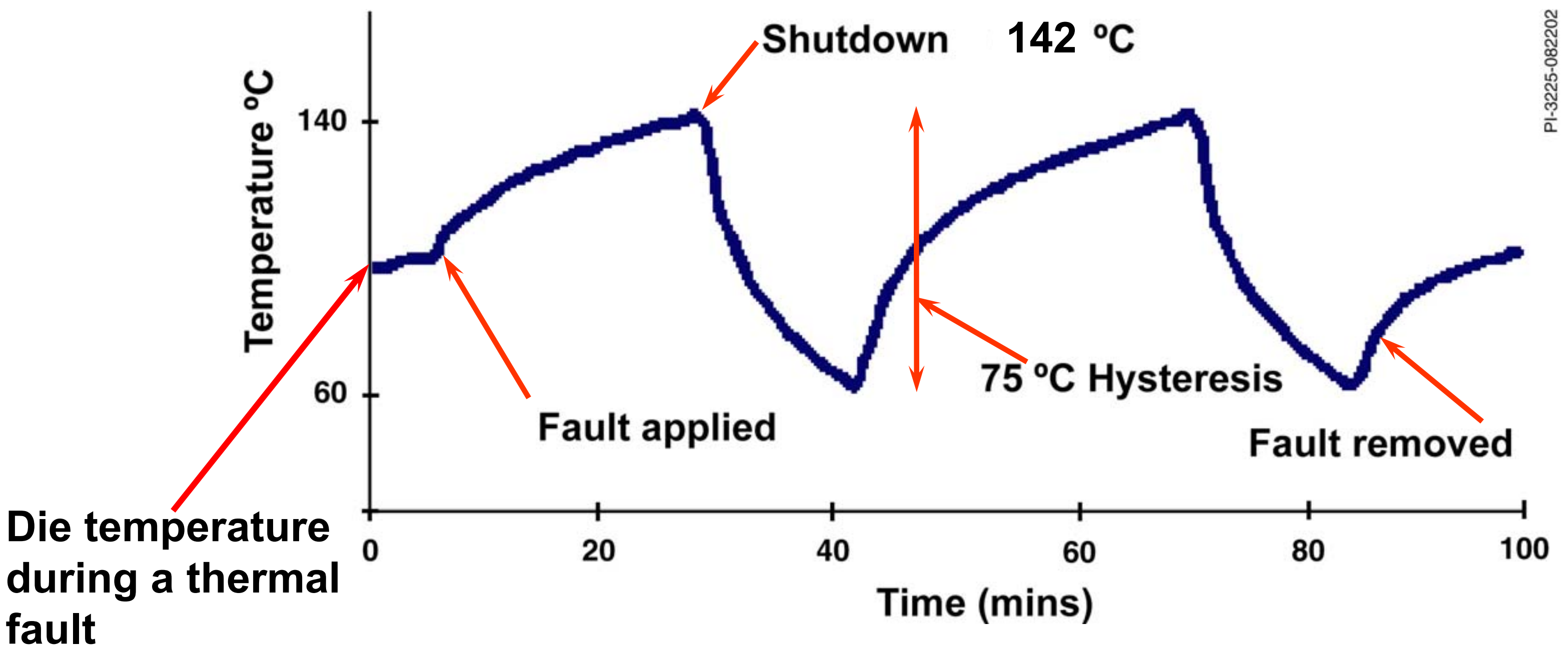
I^2f Parameter Lowers Cost

- **Increases power delivery capability**
  - Compared to designs with independent I_{LIMIT} (±7%) and f_{OSC} (±6%) tolerances:
    - Up to 5% more output power with a given core size
    - Up to 3% lower device conduction losses in a given design
- **Improves power supply manufacturability**
  - Tight tolerances improve production yields and manufacturing efficiency
- **I^2f is specified for the *TinySwitch-III* family of devices**
  - Trimmed to be within –10% to +12% at final test
  - Primary inductance calculations in the ***PI Xls*** design tool are based on I^2f

POWER INTEGRATIONS®

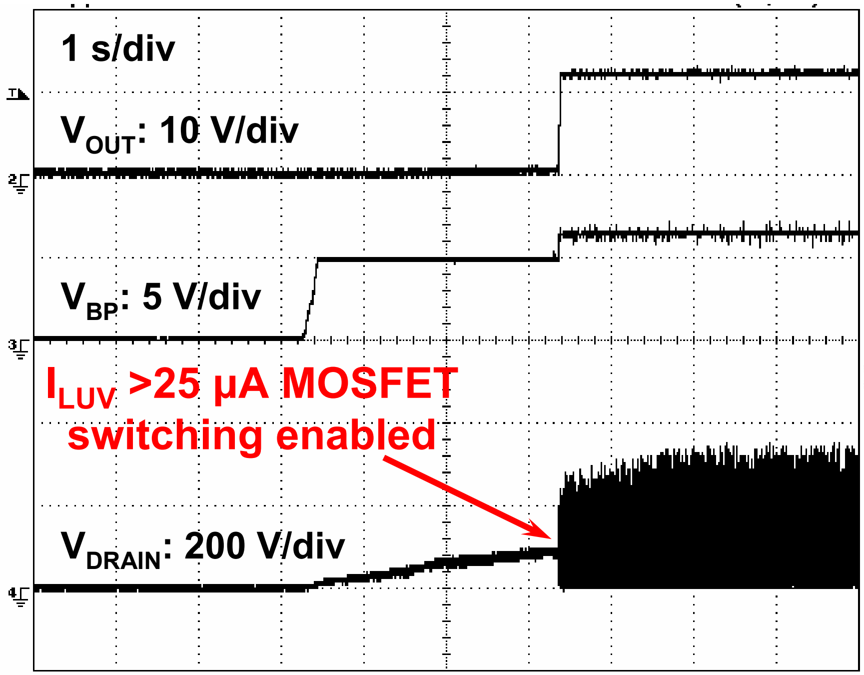
Integrated Thermal Shutdown Function

- **Accurate, integrated, hysteretic, thermal shutdown (+142 °C, ± 5%)**
  - Normal operation resumes after junction temperature drops 75 °C (hysteresis)
- **Wide hysteresis keeps average PCB temperature below 100 °C**
  - Allows use of low cost PCB material
  - Protects IC, transformer, PCB and minimizes case temperature rise

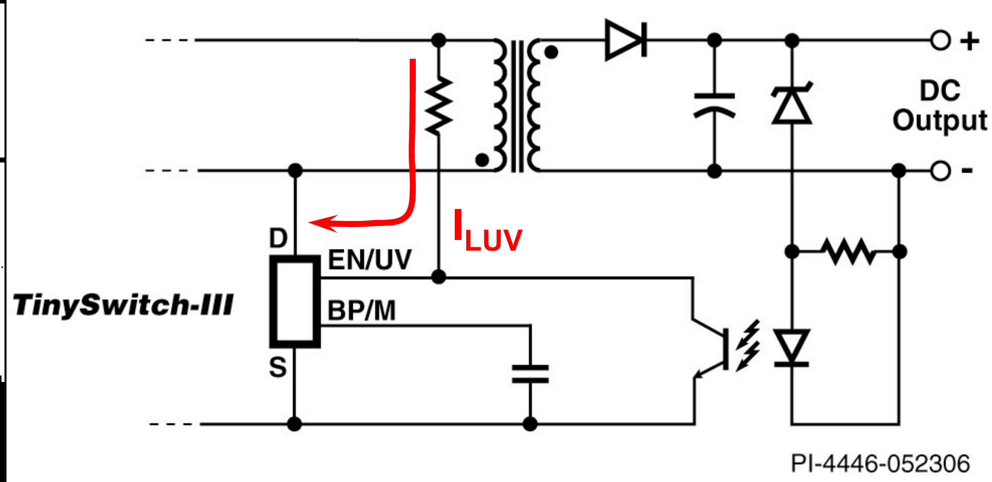


UVLO Function Prevents Output Voltage Glitches

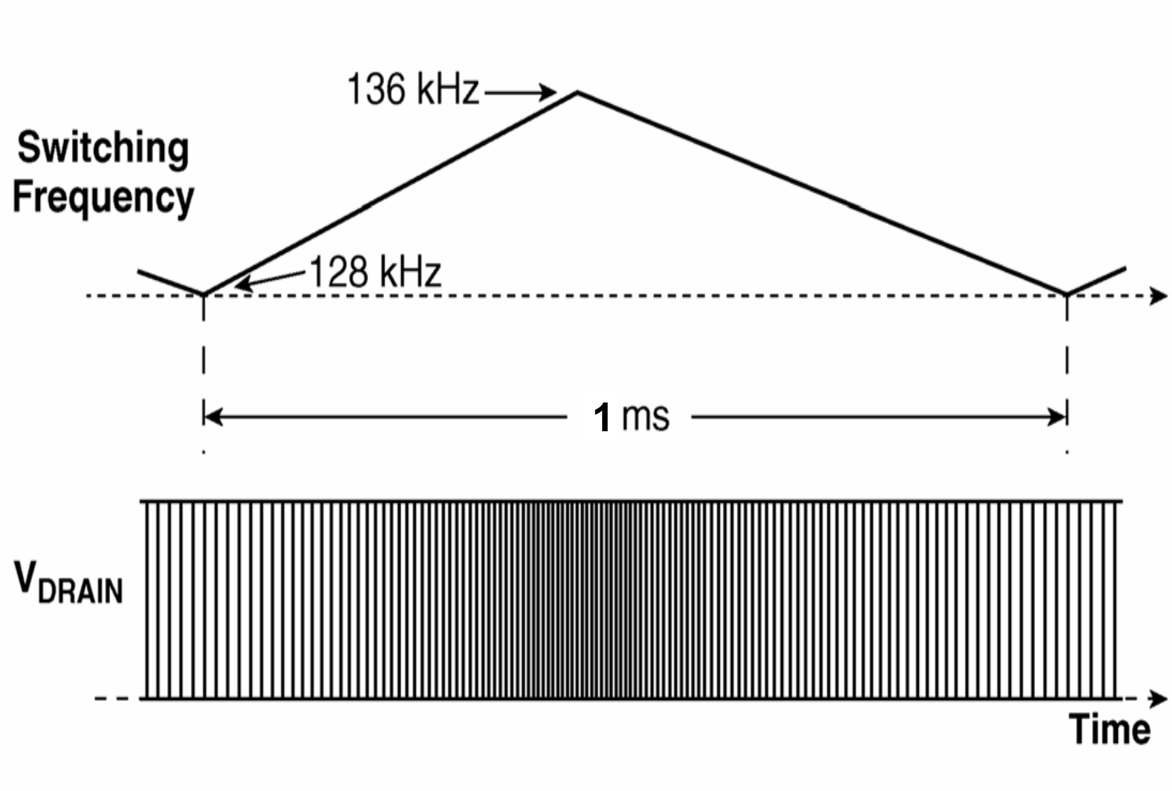
- **MOSFET switching is kept disabled until VIN reaches the UVLO threshold**
  - MOSFET switching is only enabled after EN/UV pin current (I_{LUV}) exceeds 25 μA
    - If UV resistor is absent (I_{LUV} <1 μA), the UVLO function is disabled

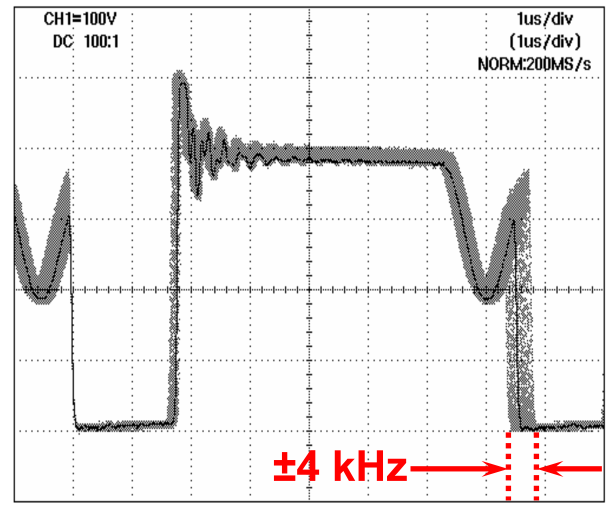


Typical waveforms during power up with a UV resistor in circuit



Switching Frequency Jitter Function



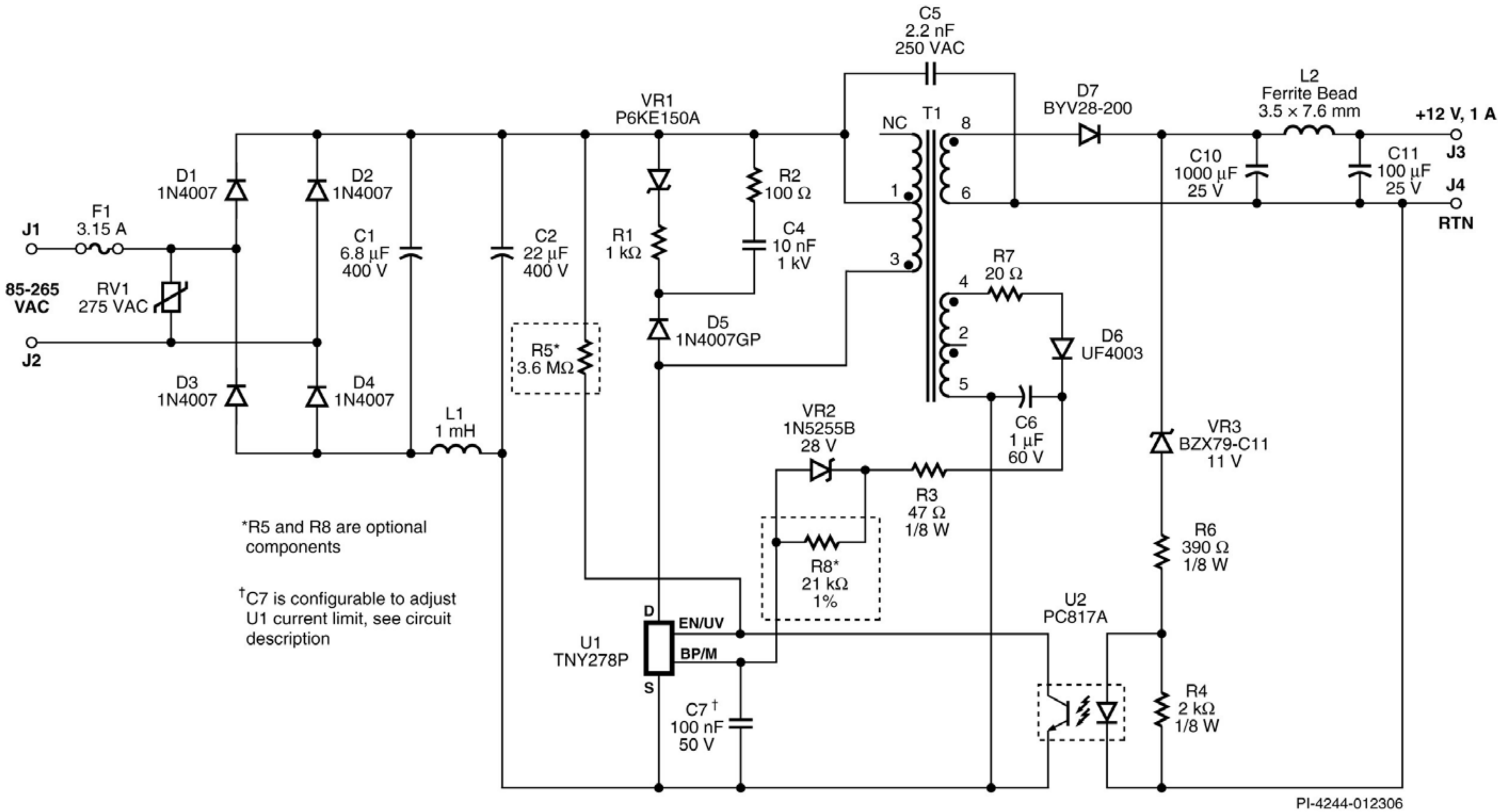


- **± 4 kHz modulation of switching frequency (at a 1 kHz rate)**
  - – Reduces size, cost and number of EMI filter components
  - – Lowers average conducted EMI up to 10 dBµV

TinySwitch-III

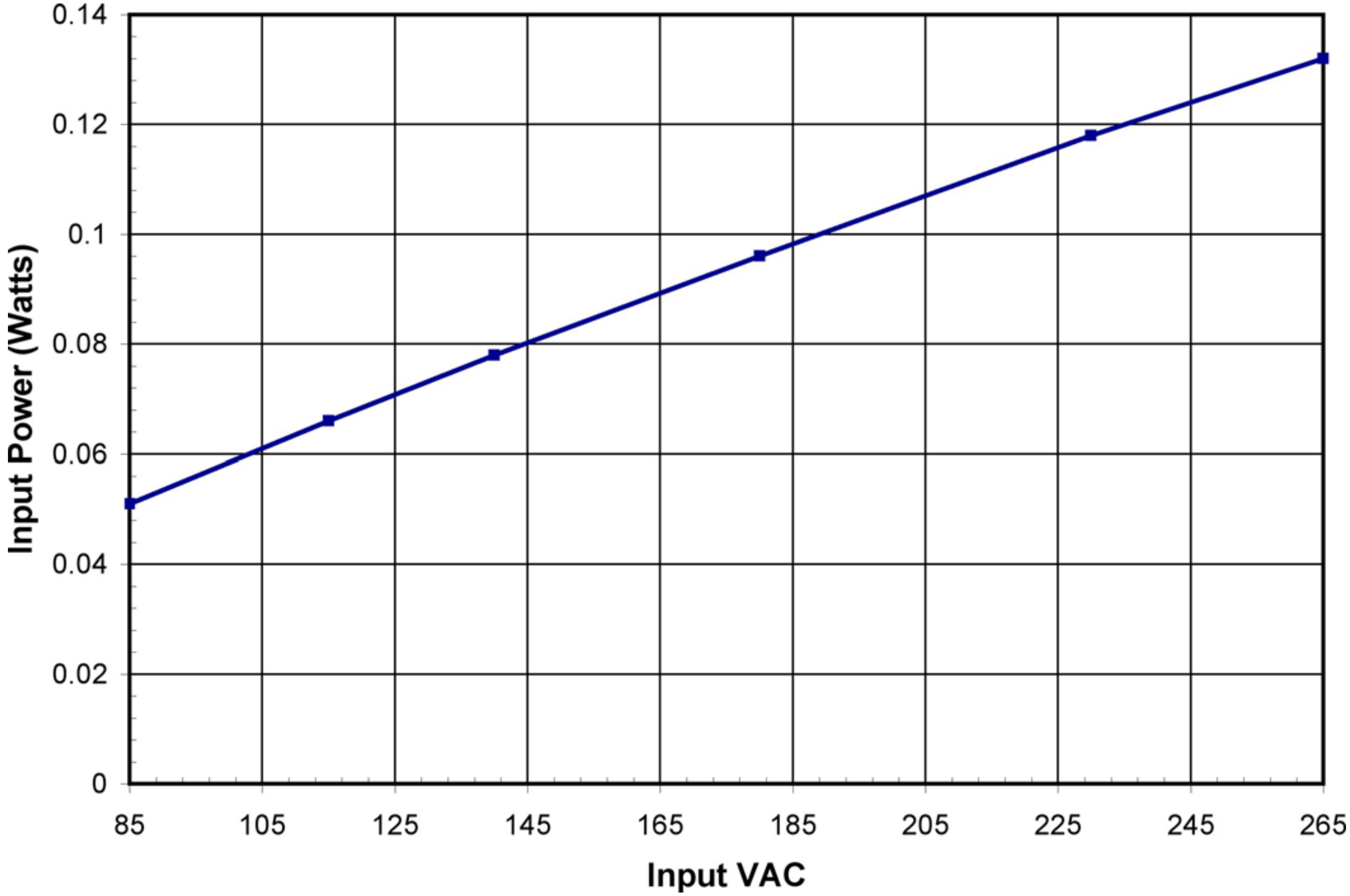
Power Supply Performance

EP-91 12 V, 12 W Universal Input Example



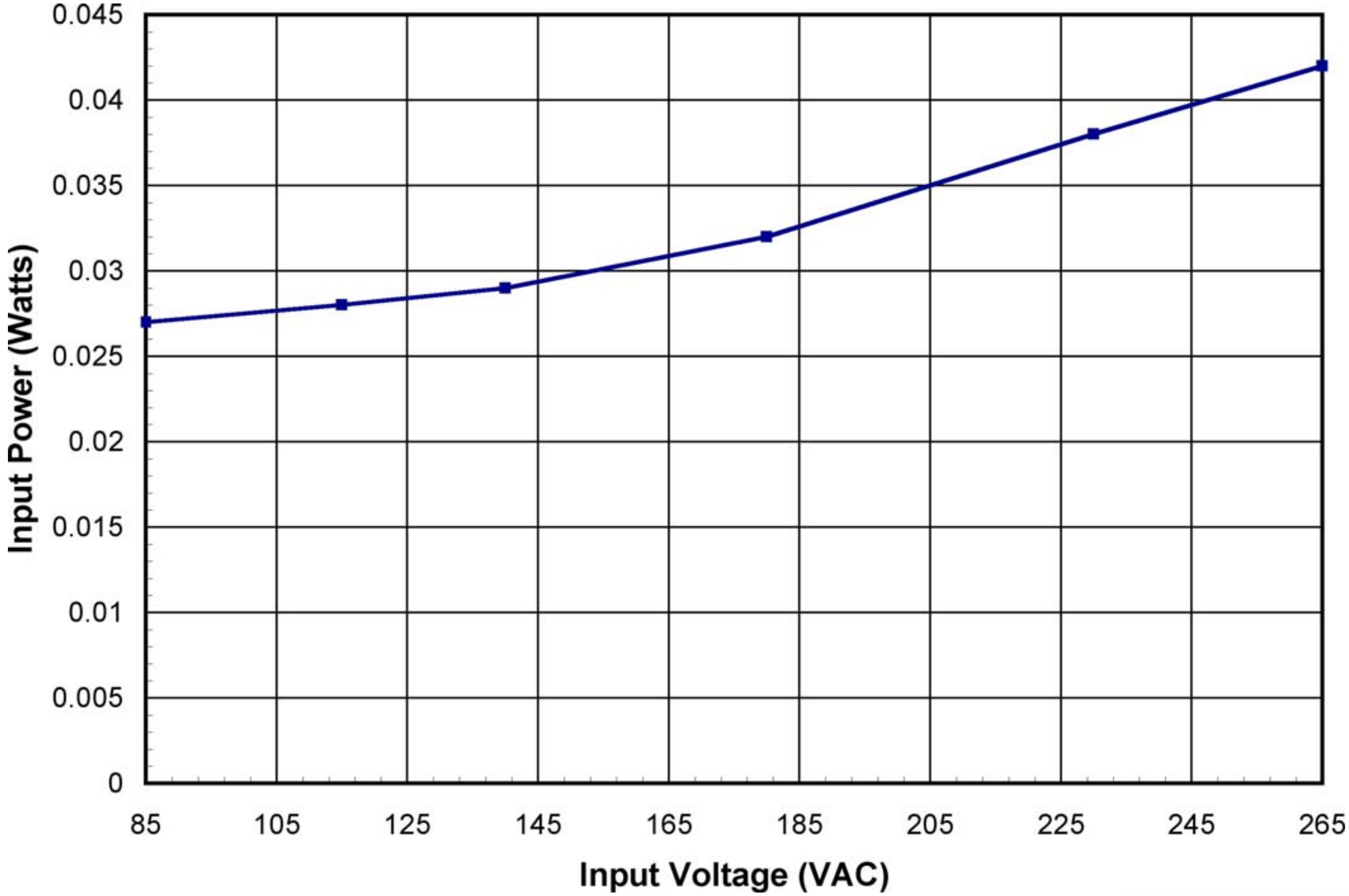
Self Biased: < 150 mW No-Load Consumption

- **IC is self powered from its internal, high-voltage current source**
  - Meets all harmonized, world-wide, no-load power consumption standards



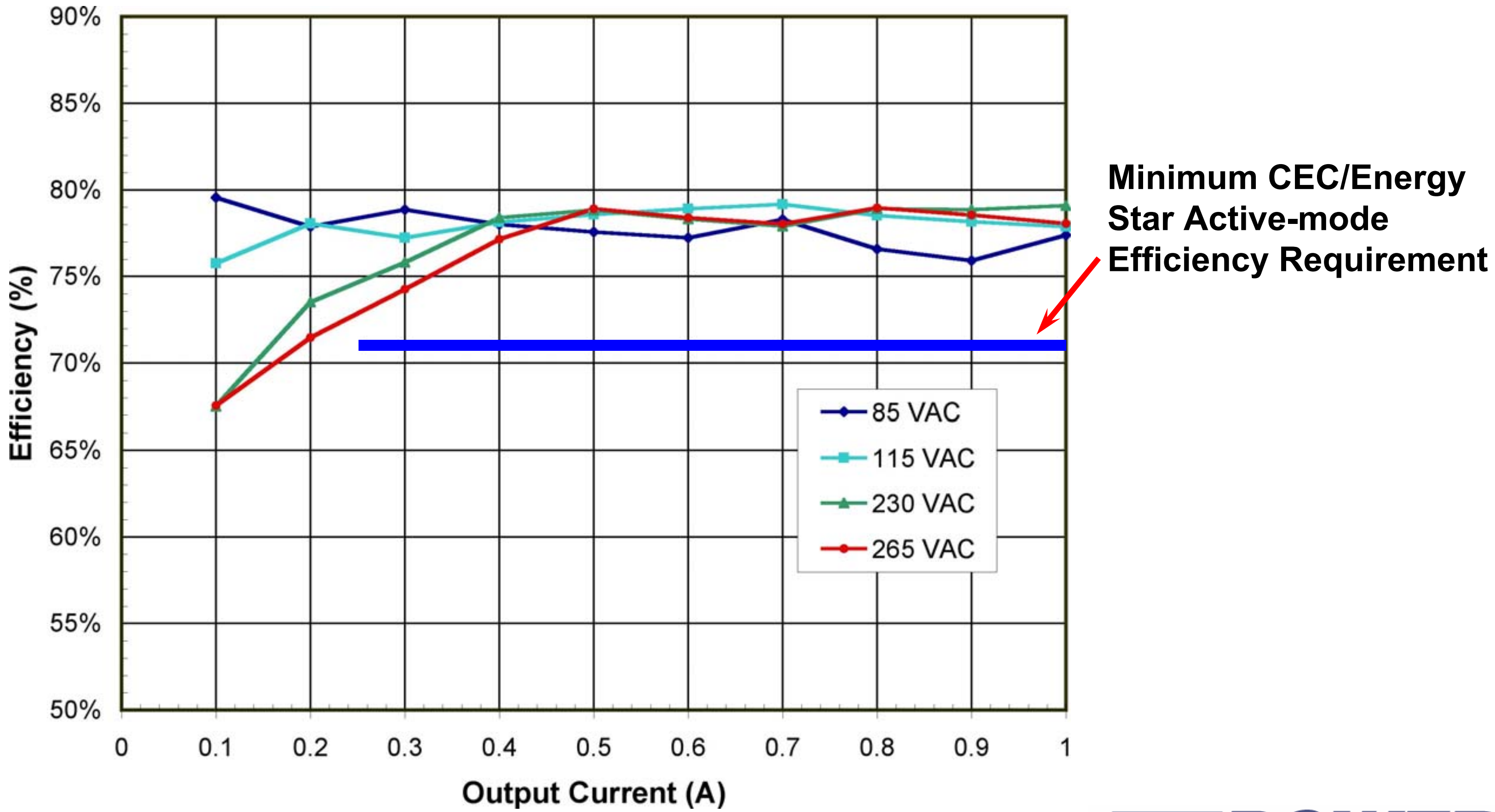
Bias Winding: < 50 mW No-Load Consumption

- **Utilizing a bias winding can reduce no-load consumption to < 50 mW**
  - Also allows implementation of OVP shutdown



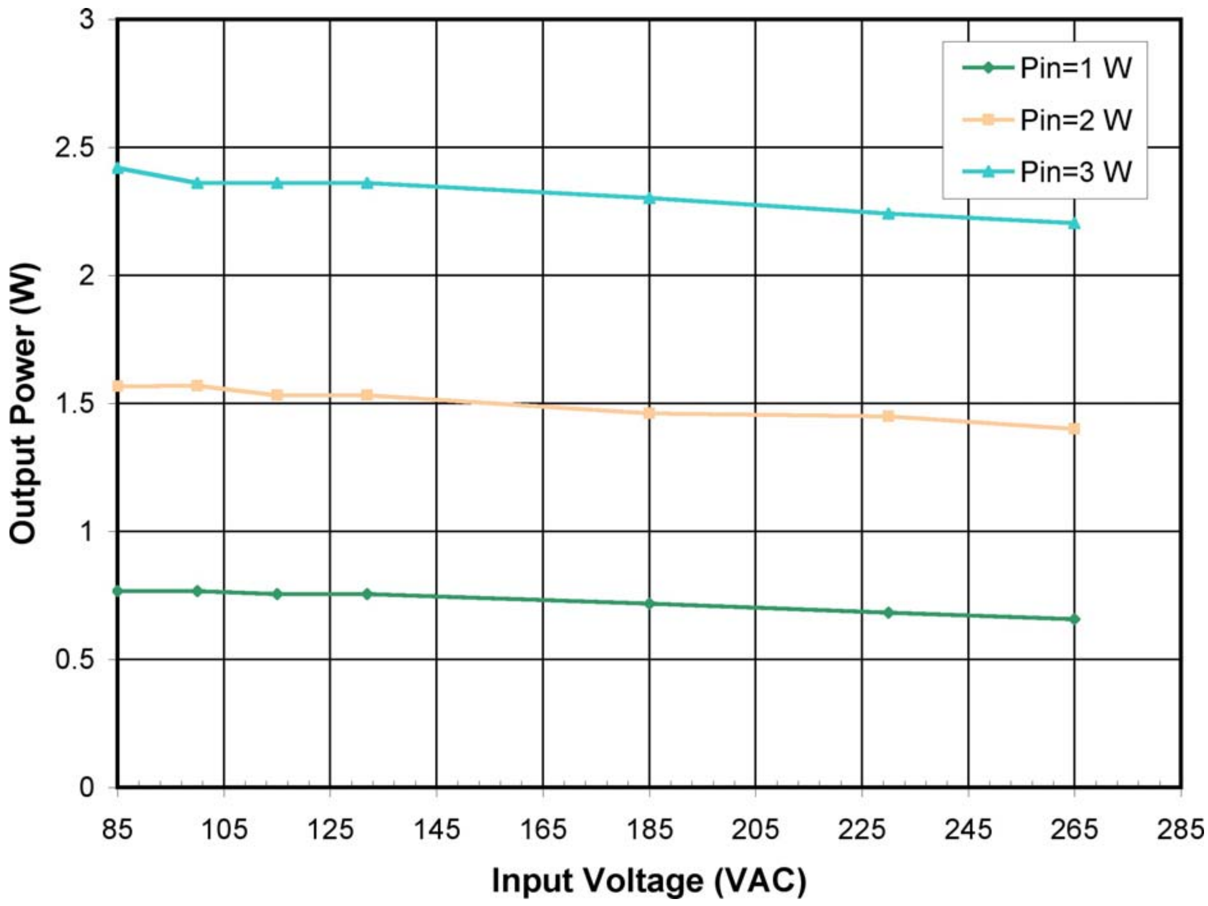
High Active Mode Efficiency

- **ON/OFF control results in consistently high efficiency across load**
  - Meets all harmonized, active-mode, energy efficiency standards

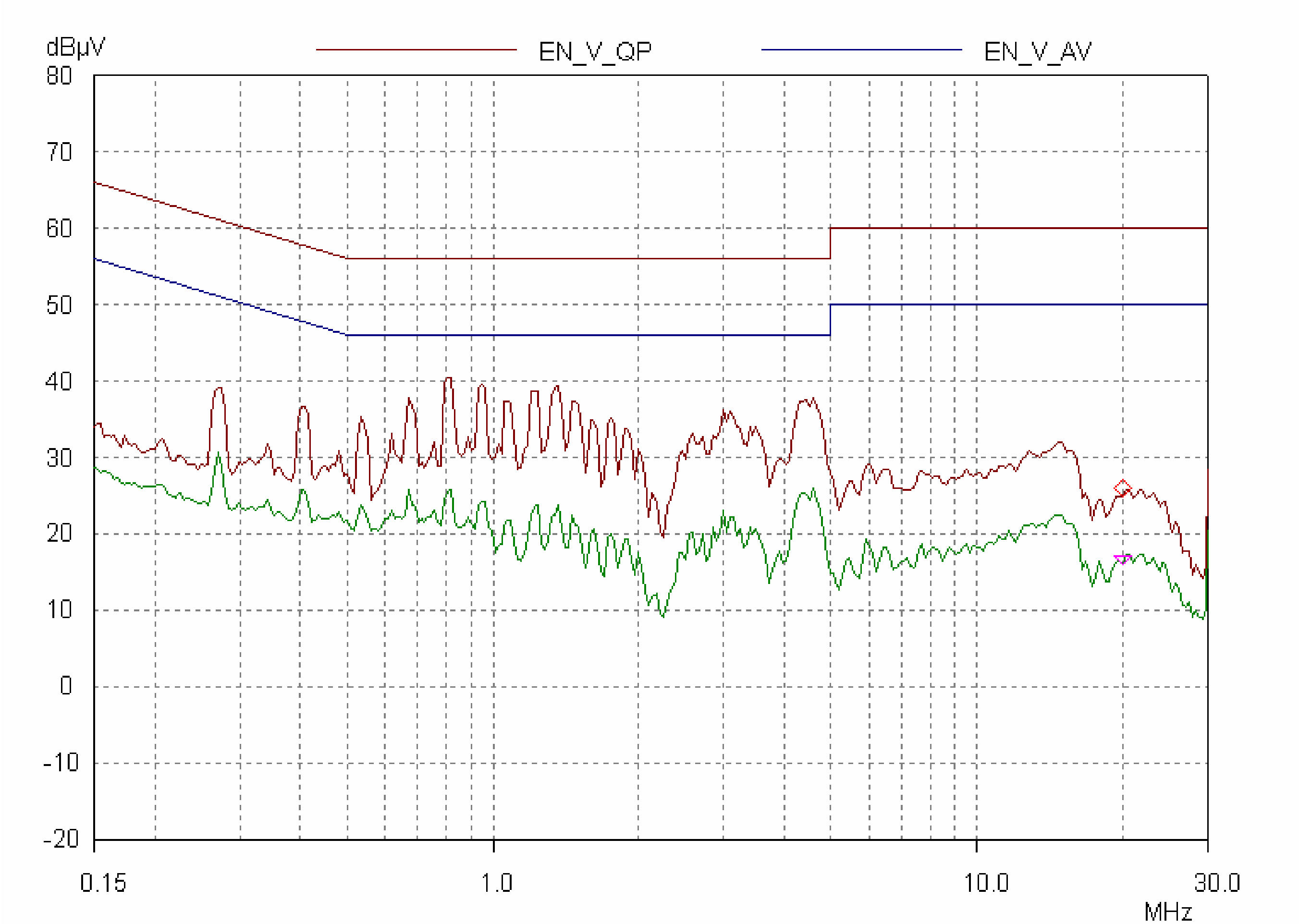


High Standby Power Availability

- **ON/OFF control keeps efficiency high in standby and sleep modes**



TinySwitch-III Conducted EMI Results



- **Worst-case measurement**
  - 230 VAC input, line measurement, artificial hand connected to output return

Designing with
TinySwitch-III

A Simple 12-Step Process

Step	Description	*PI XIs* used?
1	Choose feedback circuit type: constant voltage (CV) or constant current (CC)	No
2	Enter application variables: VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, η, Z, t_C, C_{IN}	Yes
3	Enter device variables: P/N, V_{OR}, V_{DS}, V_D	Yes
4	Enter bias winding & UVLO variables if used: V_B, V_{ZOV}, V_{UV_TARGET}, R_{UV_ACTUAL}	Yes
5	Select transformer core and bobbin (variables: A_E, L_E, A_L, BW, M, L, N_S)	Yes
6	Iterate the design (alter adjustable values) to eliminate spreadsheet warnings	Yes
7	Build transformer prototype or pass *PI XIs* outputs to a magnetics vendor	Yes
8	Select primary clamp components	No
9	Select output rectifier diode: use PIVS from spreadsheet	Yes
10	Select output capacitor(s): use IRIPPLE from spreadsheet	Yes
11	Build and test a prototype of the power supply	No
12	Use the test results to refine & document the design in the *PI XIs* spreadsheet	Yes

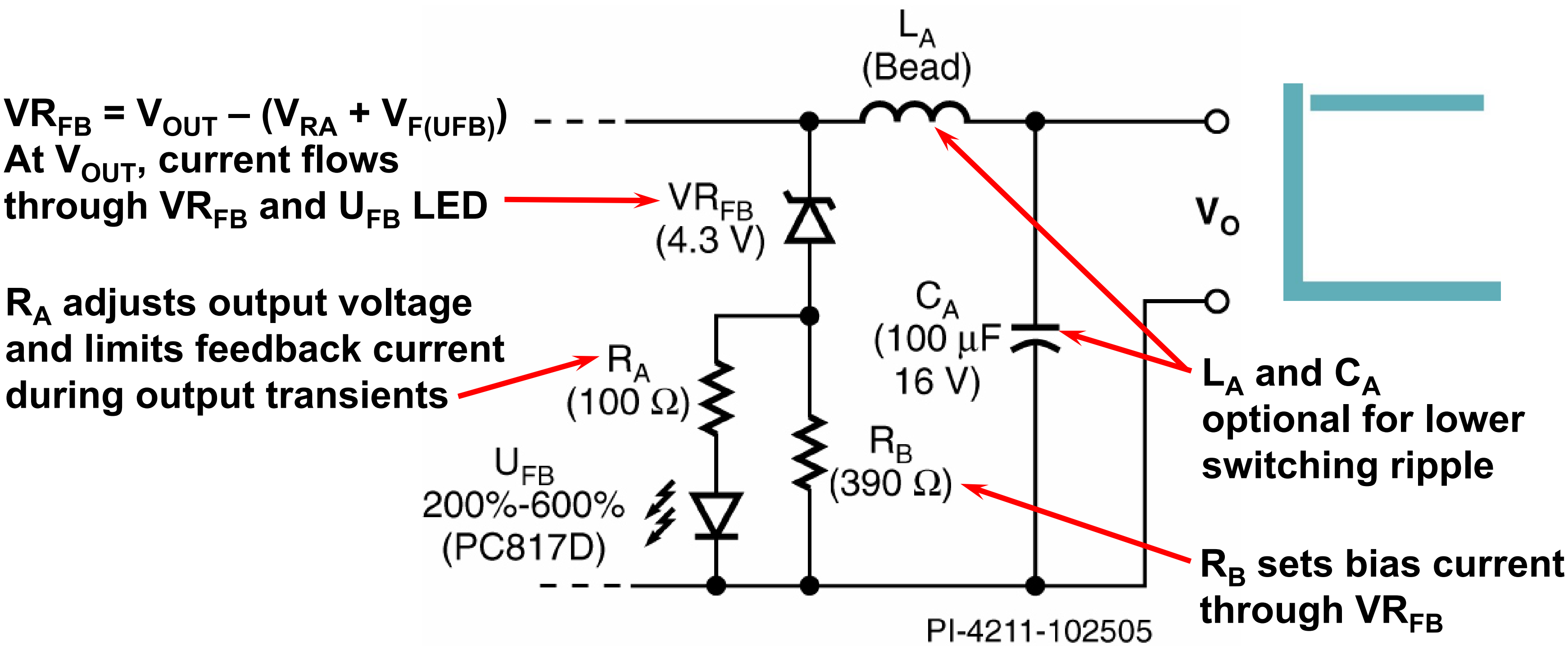
- ***PI XIs* enables engineers to quickly and easily optimize a transformer and complete a power supply design in very little time**

Step 1: Choose Feedback Circuit Type

- **Constant voltage (CV) only feedback circuits**
  - Either simple CV feedback circuit or enhanced CV feedback circuit

- **Constant voltage and constant current (CV/CC) feedback circuit**

Simple Optocoupled CV Feedback Circuit



- **Practical tolerance ± 7%, with 2%, low-current Zener (BZX79 series)**
  - Values shown in parentheses are for a 5 V output power supply

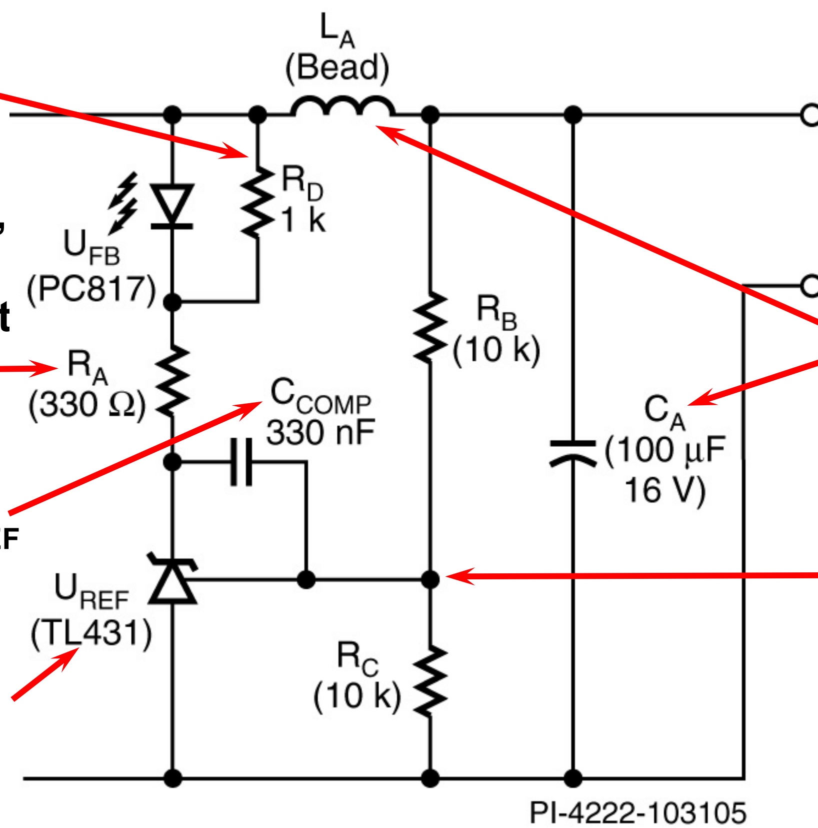
Accurate Optocoupled CV Feedback Circuit

R_D provides ≈1 mA bias for U_{REF}

R_A adjusts output voltage, sets DC gain, and limits feedback current during output load transients

C_{COMP} rolls off high frequency gain of U_{REF}

U_{REF} provides output accuracy of ±2%



L_A and C_A optional for lower switching ripple

Resistor divider R_B and R_C sets output voltage

- **U_{REF}, R_B and R_C tolerances determine accuracy of V_{OUT}**
  - Values shown in parentheses are for a 5 V output power supply

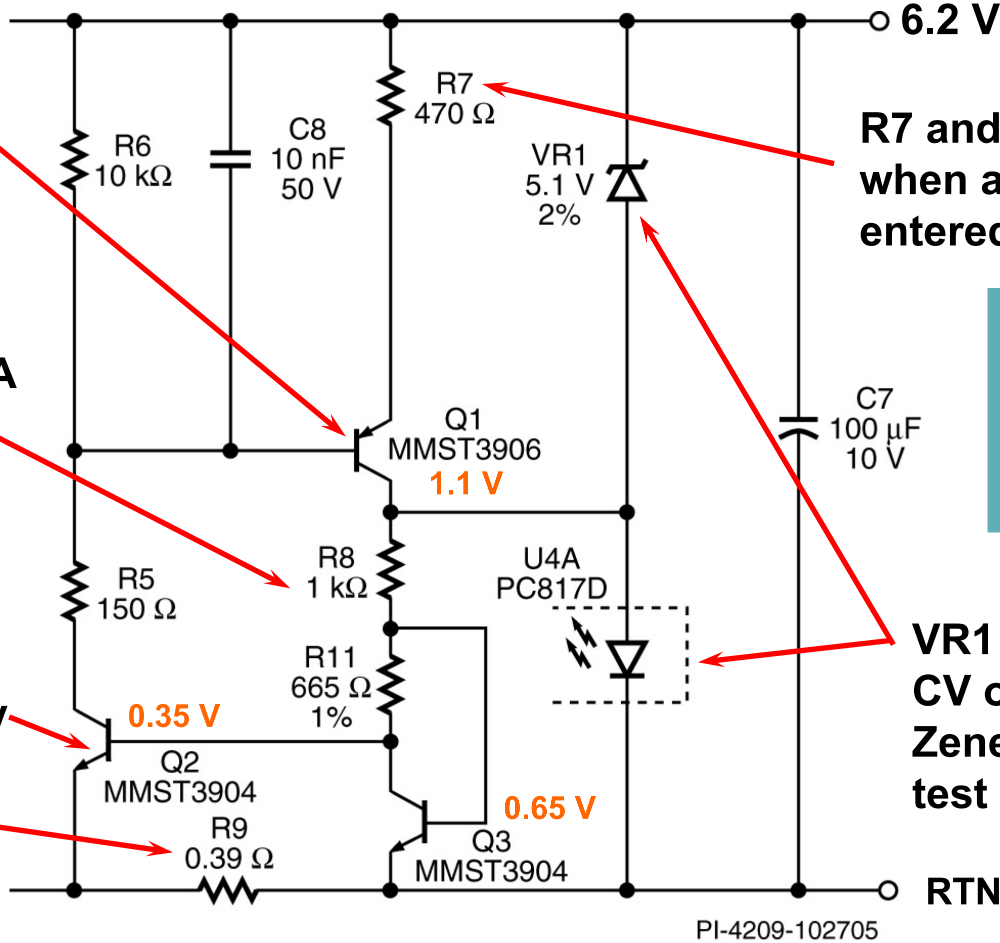
LowDrop-CC™ (0.3 V) CV/CC Feedback Circuit

At I_{OUT}, Q2 turns on, turning on Q1 and driving LED of U4A

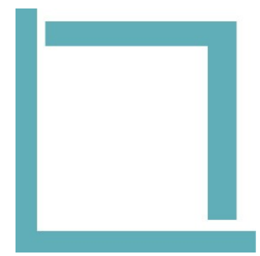
Q3, R11 and R8 bias Q2 to give 0.3 V threshold, using U4A LED as reference. Value of R11 sets threshold voltage

V_{BE} of Q2 and Q3 cancel for excellent temperature stability

R9 = 0.3 / I_{OUT}



R7 and R5 determine when auto-restart is entered (at 2 V as shown)



VR1 and U4A set CV output. Select Zener with low test current (I_{ZT})

- **Example of the value of *PI* external intellectual property**
  - This circuit can be employed with no royalty to PI when PI parts are used in the circuit

Recommended First-Pass η and Z Values

- **Efficiency (η)**
  - For constant voltage (CV) only operation, use a value of 0.75
  - For CV/CC designs with the CC threshold voltage values below (based on $V_O = 5$ V)
    - 1.1 V threshold, use 0.64
    - 0.7 V threshold, use 0.66
    - 0.3 V threshold, use 0.68

    Note: After actual efficiency has been measured on a prototype, it should be entered into the spreadsheet to refine and document the design

- **Loss Allocation Factor (Z)**
  - For opto-coupled CV only feedback, use 0.5
  - For opto-coupled CV/CC (1.1, 0.7, 0.3 V threshold), use 0.75, 0.66, 0.57 respectively

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

Step 2: Enter Variables into *PI Xls* Spreadsheet

ACDC_TinySwitch-III_020706; Rev.1.6; (c) Power Integrations 2006	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-III_020706_Rev1-6.xls; TinySwitch-III Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					Seminar Example
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (at continuous power)
IO	1.00			Amps	Power Supply Output Current (corresponding to peak power)
Power			12	Watts	Continuous Output Power
n	0.71				Efficiency Estimate at output terminals. Enter 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	33.00		33	uFarads	Input Capacitance

AC input voltage range

Line frequency

Main output voltage

Output current (increase to match total output power in multi-output designs)

Efficiency estimate

Input diode conduction time

Input capacitance

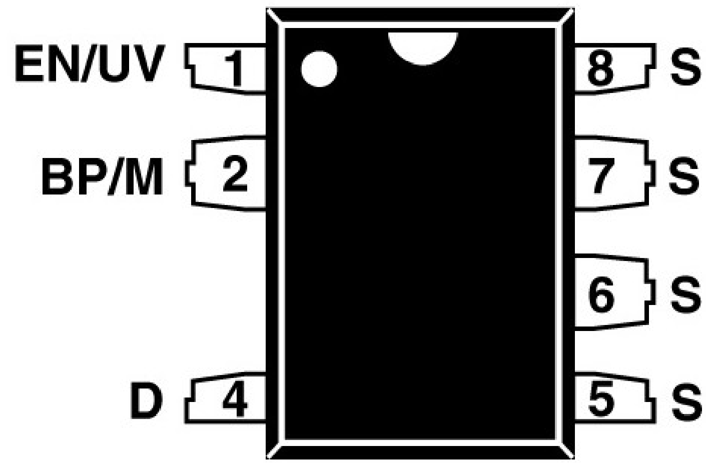
Loss allocation factor (Z): 0.5 for CV, 0.75 for CV/CC

TinySwitch-III Device Selection

OUTPUT POWER TABLE				
PRODUCT[3]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Peak or Open Frame[2]	Adapter[1]	Peak or Open Frame[2]
TNY274 P or G	6 W	11 W	5 W	8.5 W
TNY275 P or G	8.5 W	15 W	6 W	11.5 W
TNY276 P or G	10 W	19 W	7 W	15 W
TNY277 P or G	13 W	23.5 W	8 W	18 W
TNY278 P or G	16 W	28 W	10 W	21.5 W
TNY279 P or G	18 W	32 W	12 W	25 W
TNY280 P or G	20 W	36.5 W	14 W	28.5 W

Table 1. Notes: **1.** Minimum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient. Use of an external heatsink will increase power capability **2.** Minimum peak power capability in any design or minimum continuous power in an open frame design (see Key Application Considerations). **3.** Packages: P: DIP-8C, G: SMD-8C. See Part Ordering Information.

P Package (DIP-8C)
G Package (SMD-8C)



- **Actual continuous power capability depends on thermal constraints**

Step 3: Enter *TinySwitch-III* device and VOR

Enter selected *TinySwitch-III* device part number

Enter current limit choice: STD, RED, or INC

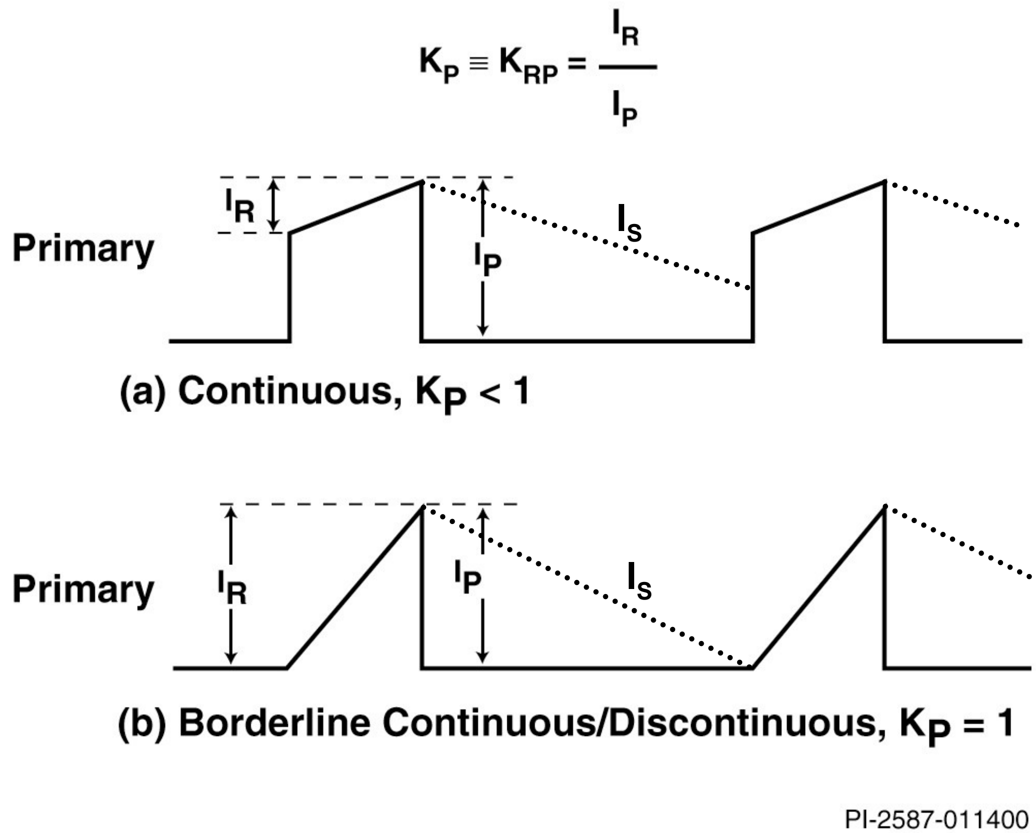
ENTER TinySwitch-III VARIABLES					
TinySwitch-III	**TNY278**		**TNY278**		User defined TinySwitch-III
Chosen Device		*TNY278*			
Chose Configuration	**STD**		Current Limit		"STD" for standard current limt or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.512	Amps	Minimum Current Limit
ILIMITTYP			0.550	Amps	
ILIMITMAX			0.588	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			35.937	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	100.00		100	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-III on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			0.64		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.38		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25

V_{OR} default value is 120 V

Output diode forward voltage drop, can be manually changed for Schottky diodes

K_P is the ripple-to-peak primary current ratio ($0.6 < K_P < 1$).
$K_{P\_TRANSIENT}$ must be ≥ 0.25 to prevent false triggering of current limit

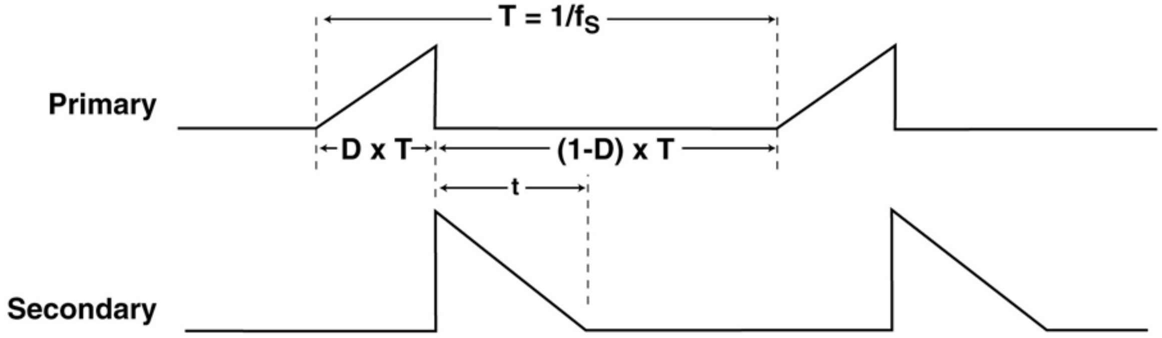
Continuous Conduction Mode (CCM) K_P



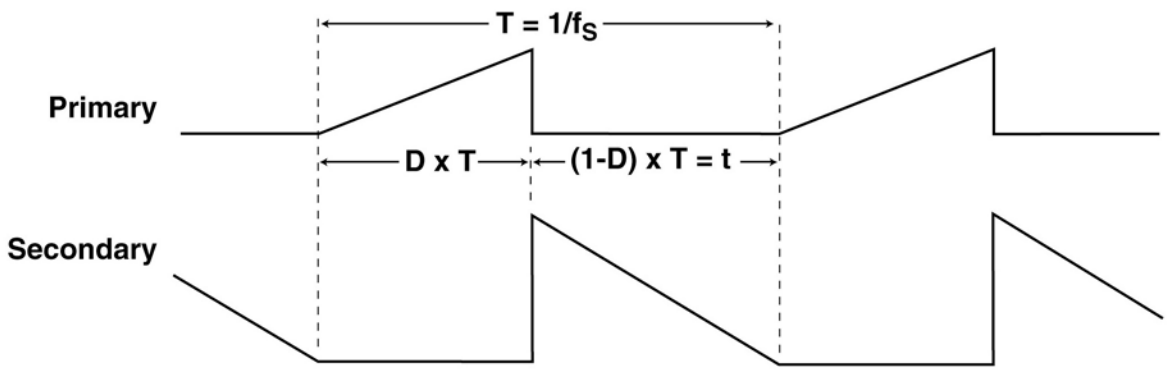
- **When the MOSFET switch turns on before the secondary current has reduced to zero, the supply is operating in CCM**

Discontinuous Conduction Mode (DCM) K_P

$$K_P \equiv K_{DP} = \frac{(1-D) \times T}{t}$$



(a) Discontinuous, $K_P > 1$



(b) Boarderline Discontinuous/Continuous, $K_P = 1$

PI-2578-011800

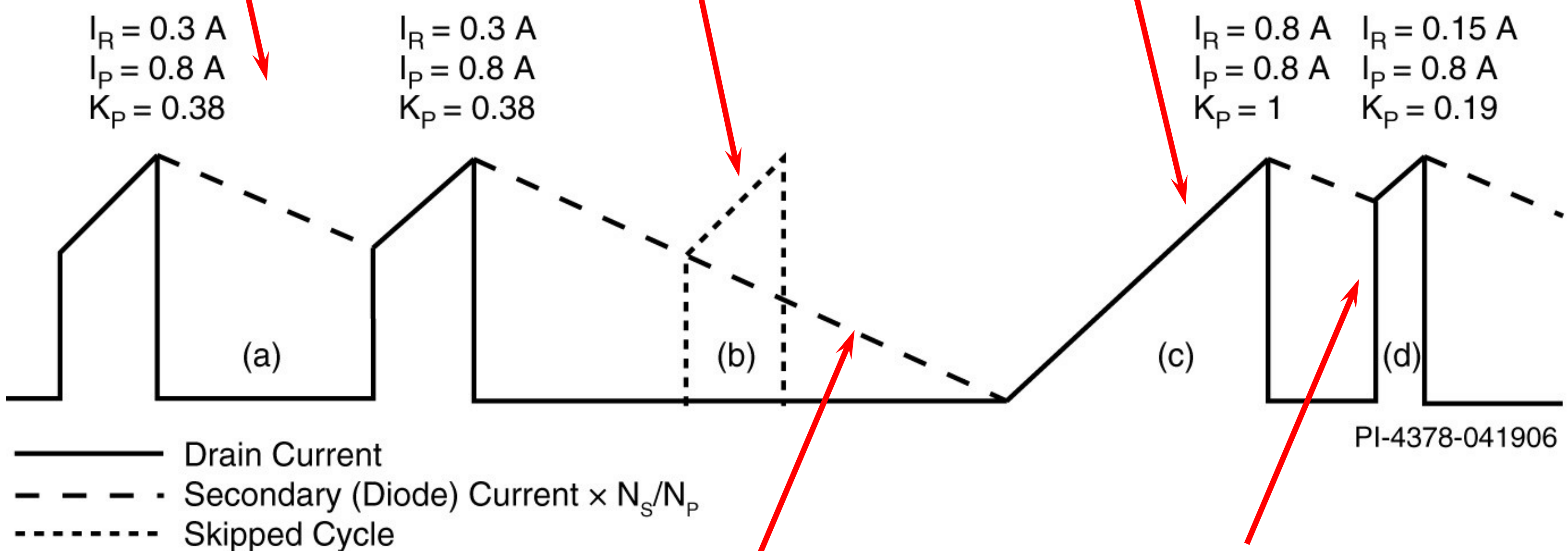
- **In DCM, secondary current is zero when the MOSFET turns on**

Transient vs Steady State K_P

Steady state switching cycle sequence (a)

Feedback requires a skipped cycle (b)

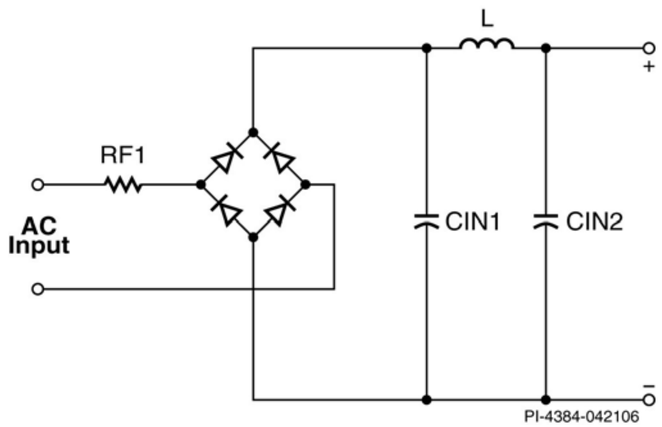
On-time of next enabled cycle longer as primary current ramps from zero (c)



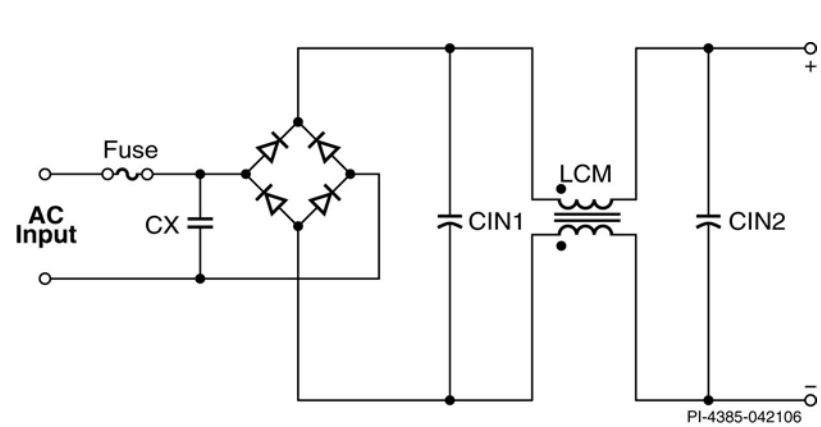
Secondary current ramps to zero: all energy in transformer delivered to load (b)

Reduced off-time of following cycle causes much lower transient K_P value (d)

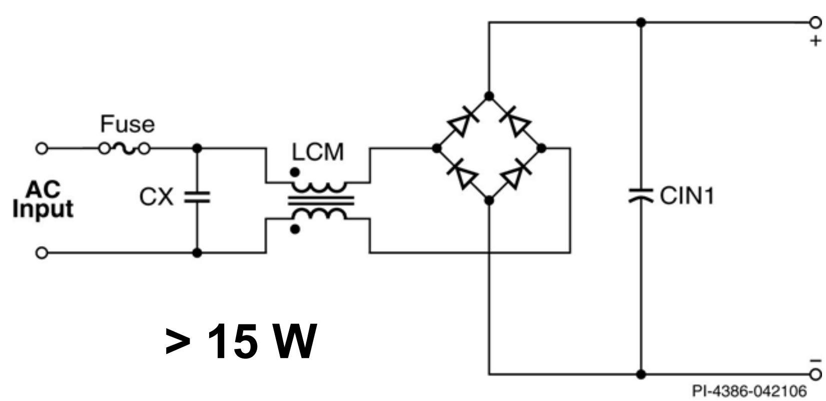
Input Stage Selection



4 W to 10 W



10 W to 15 W



> 15 W

Input Capacitance Value

Total Input Capacitance Required	
AC Input Voltage	μF per Watt of Output Power
85–265	2 to 3
100/115	2 to 3
230	1

- **Check rectified input voltage V_{MIN} at low-line (AC input) and full load**
  - V_{MIN} should be ≥ 70 VDC
    - *PI XIs* calculates the minimum input capacitance value for V_{MIN} ≥70 VDC
- **On-time extension feature minimizes value of C_{IN}**
  - Maximizes energy delivery and holdup time during power down and brownout

Step 4: Enter Bias Winding and UVLO Variables

A user specified bias winding voltage can be entered in the over-ride cell

ENTER BIAS WINDING VARIABLES				
VB		22.00	Volts	Bias Winding Voltage
VDB		0.70	Volts	
NB		6.93		Bias Winding Number of Turns
VZOV		28.00	Volts	Over Voltage Protection zener diode.
UVLO VARIABLES				
V_UV_TARGET		93.85	Volts	Target under-voltage threshold, above which the power supply with start
V_UV_ACTUAL		92.20	Volts	Typical start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL		3.67	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL		3.60	Mohms	Closest standard value of resistor to RUV_IDEAL

Entering resistor value will calculate the actual UV voltage

Enter specific target value of the DC input startup voltage

Enter the value of the Zener diode if it differs from the calculated value

- **A bias voltage of 22 V and a 28 V Zener gives good OVP performance**
  - For 12 V output, OVP limits peak voltage to ≈15 V during open loop fault

POWER INTEGRATIONS

Step 5: Select Transformer Core and Bobbin

Select the desired core from drop down menu

Grey, over-ride cells can be used to enter custom core / bobbin types

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EF20**		**EF20**		User-Selected transformer core
Core		*EF20*		*P/N:*	PC40EF20-Z
Bobbin		*EF20_BOBBIN*		*P/N:*	EF20_BOBBIN
AE			0.335	cm^2	Core Effective Cross Sectional Area
LE			4.49	cm	Core Effective Path Length
AL			1570	nH/T^2	Ungapped Core Effective Inductance
BW			12.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3		Number of Primary Layers
NS			6		Number of Secondary Turns

Enter half of total required margin (enter 3 mm for 6 mm total margin)

The number of secondary turns are calculated to keep the flux density < 3000 Gauss (300 mT). Other values can be entered in over-ride cell.

Enter number of primary winding layers (L ≤ 4) if different from that calculated by *PI Xls*

Step 6: Iterate Design to Eliminate Warnings

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			966	uHenries	Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 862 uH
LP_TOLERANCE			12	%	Primary inductance tolerance
NP			38		Primary Winding Number of Turns
ALG			676	nH/T^2	Gapped Core Effective Inductance
BM		*Warning*	4485	Gauss	!!! Warning. Maximum flux density too high, may cause transformer saturation. REDUCE BP<3000. Increase NS > 6
BAC			1661	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1675		Relative Permeability of Ungapped Core
LG		*Warning*	0.04	mm	!!! INCREASE GAP>>0.1 (increase NS, increase VOR,bigger Core
BWE			36.6	mm	Effective Bobbin Width
OD			0.97	mm	Maximum Primary Wire Diameter including insulation
INS			0.08	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.89	mm	Bare conductor diameter
AWG			20	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			1024	Cmils	Bare conductor effective area in circular mils
CMA		*Info*	3341	Cmils/Amp	CAN DECREASE CMA < 500 (decrease L (primary layers), increase NS, use smaller core)

- **Follow *PI XIs* guidance in comments column to bring design within acceptable best practice limits**

Step 6a: Iterating Design Details

- **VOR recommendations**
  - Highest efficiency typically occurs with a VOR value of:
    - 90-110 V for 85-265 VAC (universal) input (or multiple outputs)
    - 120-135 V for 185-265 VAC (single) input
  - A value of 135 V delivers maximum power from a given device
- **Relationship between primary layers (L), secondary turns (N_S), core size, flux density (B_M), core gap (L_g) and current density (CMA)**

		B_M	L_g	CMA
L	↑	-	-	↑
N_S	↑	↓	↑	↓
core size	↑	↓	↑	↑

↑= Value increases

↓= Value decreases

- = No change

Key Outputs From *PI XIs* Spreadsheet

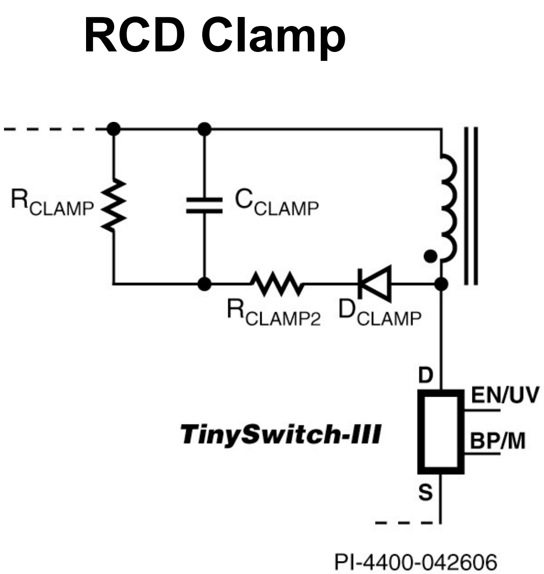
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			966	uHenries	Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 862 uH
LP_TOLERANCE			12	%	Primary inductance tolerance
NP			57		Primary Winding Number of Turns
ALG			300	nH/T^2	Gapped Core Effective Inductance
BM			2990	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1107	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1675		Relative Permeability of Ungapped Core
LG			0.11	mm	Gap Length (Lg > 0.1 mm)
BWE			24.4	mm	Effective Bobbin Width
OD			0.43	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.37	mm	Bare conductor diameter
AWG			27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			203	Cmils	Bare conductor effective area in circular mils
CMA		*Info*	663	Cmils/Amp	CAN DECREASE CMA < 500 (decrease L (primary layers), increase NS, use smaller core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			4.84	Amps	Peak Secondary Current
ISRMS			2.29	Amps	Secondary RMS Current
IRIPPLE			2.07	Amps	Output Capacitor RMS Ripple Current
CMS			459	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			23	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			647	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			52	Volts	Output Rectifier Maximum Peak Inverse Voltage

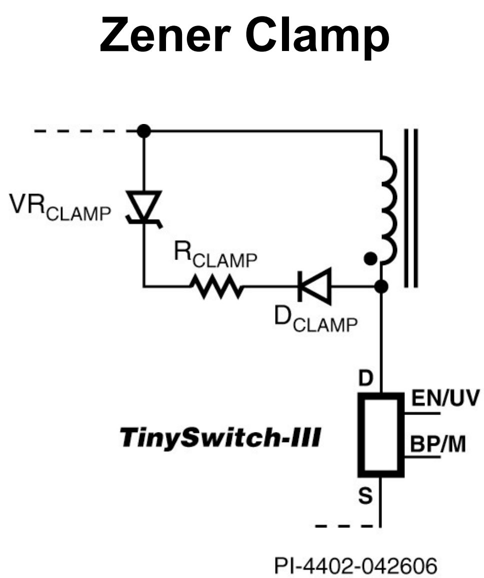
- **Provides key information for component selection and transformer design**

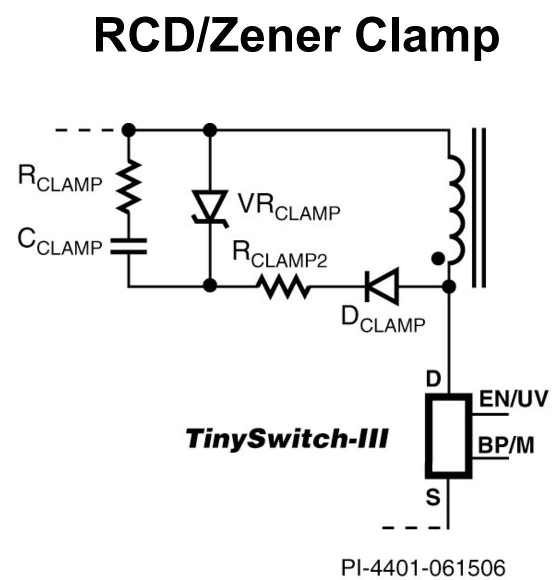
Step 7: Use *PI XIs* Outputs to Build A Transformer Prototype

- **All data needed to build a transformer prototype is provided, such as:**
  - Primary Inductance L_P
    - default tolerance ±12 %, adjust based on vendor input
  - Core gap length (L_g) and gapped core effective inductance (A_{LG}) values
  - Number of primary, secondary and bias winding turns (N_P, N_S and N_B)
  - Wire diameter sizes for each winding
- ***PI XIs* helps in selecting other *TinySwitch-III* support components by calculating:**
  - Output capacitor ripple current (I_{RIPPLE}) value
  - Output diode reverse voltage stress value
  - Zener diode voltage for OVP implementation
  - UVLO resistor value

Step 8: Primary Clamp Component Selection







MOSFET Drain Clamp	RCD	Zener	RCD / Zener
Component cost	Lowest	Higher	Highest
No-load input power	Highest	Lowest	Low
Light-load efficiency	Lowest	Highest	High
EMI generation	Lowest	Highest	Low

Step 9: Output Diode Selection

Series Number	***Type***	***$V_{REVERSE}$ Range (V)***	***Forward Current (A)***	***Package***	***Manf***
SB120 – 1100	Schottky	20–100	1	Axial Lead	Vishay
SB320 – 3100	Schottky	20–100	3	Axial Lead	Vishay
SB520 – 5100	Schottky	20–100	5	Axial Lead	Vishay
MBR735 – 745	Schottky	35–45	7.5	TO-220AC	Vishay
MBR1045 – 1060	Schottky	45–60	10	TO-220AC	Vishay
MBR2045CT	Schottky	45	20	TO-220AB	Vishay
UF4002 – 4006	Ultrafast	100–600	1	Axial Lead	Vishay
UF5401 – 5408	Ultrafast	100–800	3	Axial Lead	Vishay
MUR620	Ultrafast	200	6	TO-220AB	On Semi
MUR820 – 840	Ultrafast	200–400	8	TO-220AC	On Semi
ES2A – ES2D	Ultrafast	50–200	2	SMD	Vishay

- **Sample Schottky and Ultrafast diodes for use in *TinySwitch-III* designs**
  - Output diode current rating should be ≥ rated output current

Step 10: Output Capacitor Selection

- **Capacitor voltage rating should be > 1.25 × V_O**
- **Capacitor ripple current rating should be > I_{RIPPLE}**
  - Output capacitor I_{RIPPLE} ratings are inversely proportional to temperature
    - Example: A 105°C capacitor working at 85°C has an I_{RIPPLE} factor of 1.7
    - Check manufacturer's datasheet for specific factors

Voltage (V)	*Value* (μF)	I_{RIPPLE} (A) (at rated life, 105°C)	*UCC Series*	*Size* (dxl mm)	
10 V	470	0.76	KZE	8 x 11.5	
10 V	1000	1.25	KZE	8 x 20	← **typical 5 V, 6 W design**
10 V	1500	2.15	KZE	10 x 25	
16 V	470	1.03	KZE	10 x 12.5	
16 V	1000	1.82	KZE	10 x 20	← **typical 12 V, 15 W design**
25 V	470	1.25	KZE	8 x 20	
25 V	1000	2.36	KZE	12.5 x 20	
35 V	330	1.43	KZE	10 x 16	
35 V	470	1.82	KZE	10 x 20	
50 V	220	1.37	KZE	10 x 16	
50 V	330	1.87	KZE	10 x 25	
63 V	100	0.535	LXZ	8 x 15	
63 V	220	1.05	LXZ	10 x 25	

Steps 11–12: Test Prototype & Refine Design

- **Build and test prototype of power supply**
- **Measure peak drain voltage at maximum input voltage, the minimum DC bus voltage (V_{MIN}) and efficiency at low line**
- **Verify that V_{MIN} is ≥70 V**
  - Increase input capacitance value if necessary
- **Verify peak drain voltage <650 V at maximum line voltage**
- **Enter measured parameters into the *PI Xls* spreadsheet**
  - Efficiency (η)
  - Measured value of V_{MIN}

TinySwitch-III Design Tools

- **Reference Design (Design Accelerator Kit) DAK-91:**
  - Built and tested 12 W power supply (EP-91)
  - Engineering report (EPR-91)
  - Blank PCB and IC samples
  - *PI Expert* Suite power supply design software
  - Datasheet
  - Design Idea DI-91

TinySwitch-III

Hints and Tips

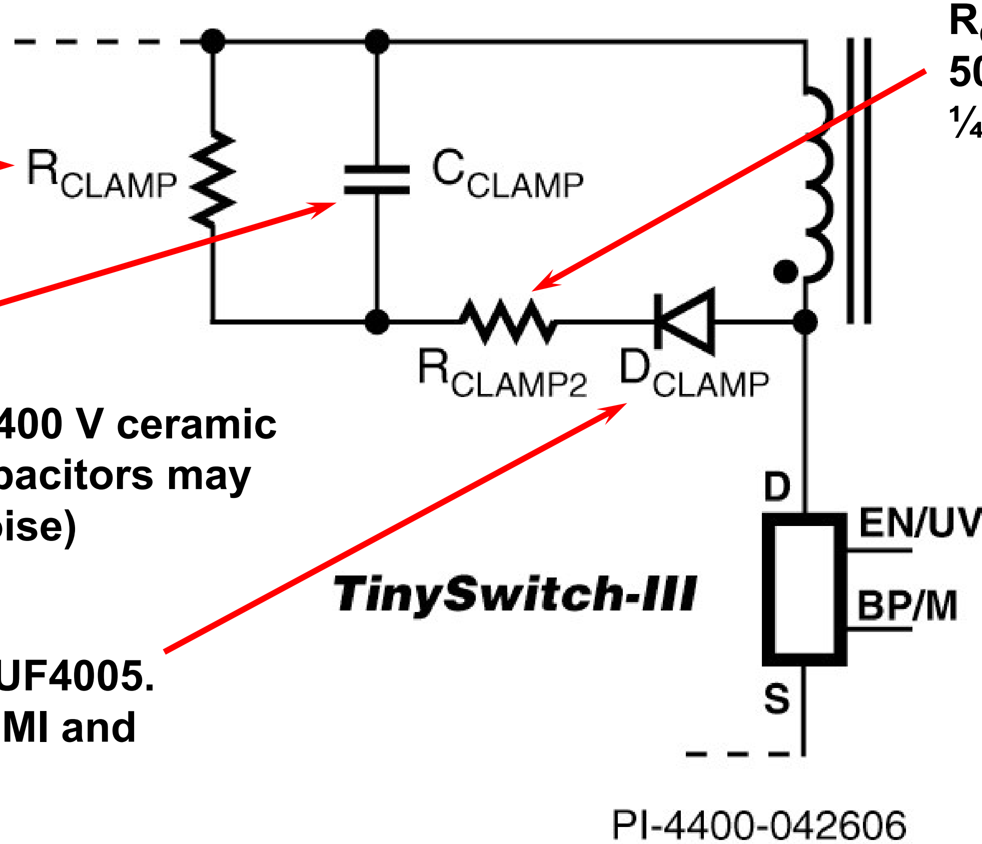
Low-cost RCD Clamp Circuit

R_{CLAMP}:
47 kΩ to 200 kΩ,
½ W to 3 W

C_{CLAMP}:
330 pF to 3.3 nF, ≥ 400 V ceramic or film (ceramic capacitors may produce audible noise)

D_{CLAMP}:
FR107, 1N4937, or UF4005.
FR107 gives best EMI and efficiency

R_{CLAMP2}:
50 Ω to 330 Ω,
¼ W



- **For applications where lowest cost and EMI are most important**

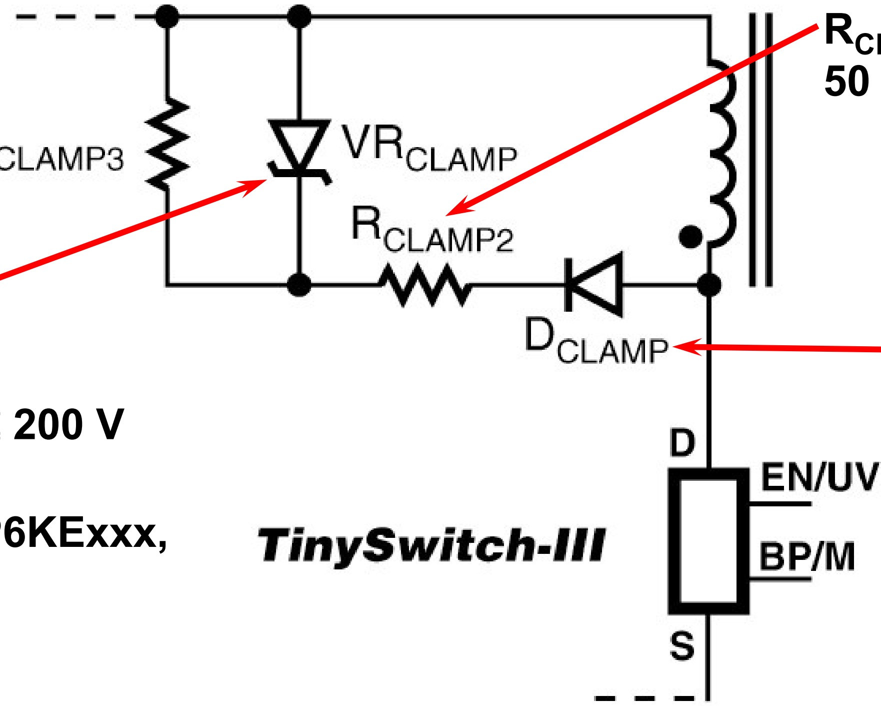
Low-cost RCD Clamp Design Guidelines

- **Minimize value of C_{CLAMP} and maximize value of R_{CLAMP}**
  - Maximizes efficiency and minimizes no-load input power consumption
  - Reduce value of R_{CLAMP} to improve conducted EMI in the 1-2 MHz region
    - Increases damping of leakage inductance ringing
  - Dissipation of $P_{RCLAMP} = V_{CCLAMP}^2 / R_{CLAMP}$
    - Measure voltage across C_{CLAMP} at full load, low line using a DVM
    - Select suitable resistor power rating
- **R_{CLAMP2} dampens ringing when a 500 ns diode (FR107) is used**
- **Keep V_{DRAIN} < 650 V to provide margin for unit-to-unit variation**

High-Efficiency Zener Clamp Circuit

R_{CLAMP3}:
Optional to reduce zener dissipation and EMI
47 kΩ to 330 kΩ

VR_{CLAMP}:
$1.4 \times V_{OR} \leq VR_{CLAMP} \leq 200$ V
0.5 W to 1 W rating
Part number series P6KExxx, BZY97Cxxx, BZX55



PI-4402-060806

R_{CLAMP2}:
50 Ω to 330 Ω, ¼ W

D_{CLAMP}:
FR107, 1N4937 or UF4005.
FR107 gives best EMI and efficiency

- **For applications where lower no-load consumption and higher light load efficiency are most important**

High-Efficiency Zener Clamp Design Guidelines

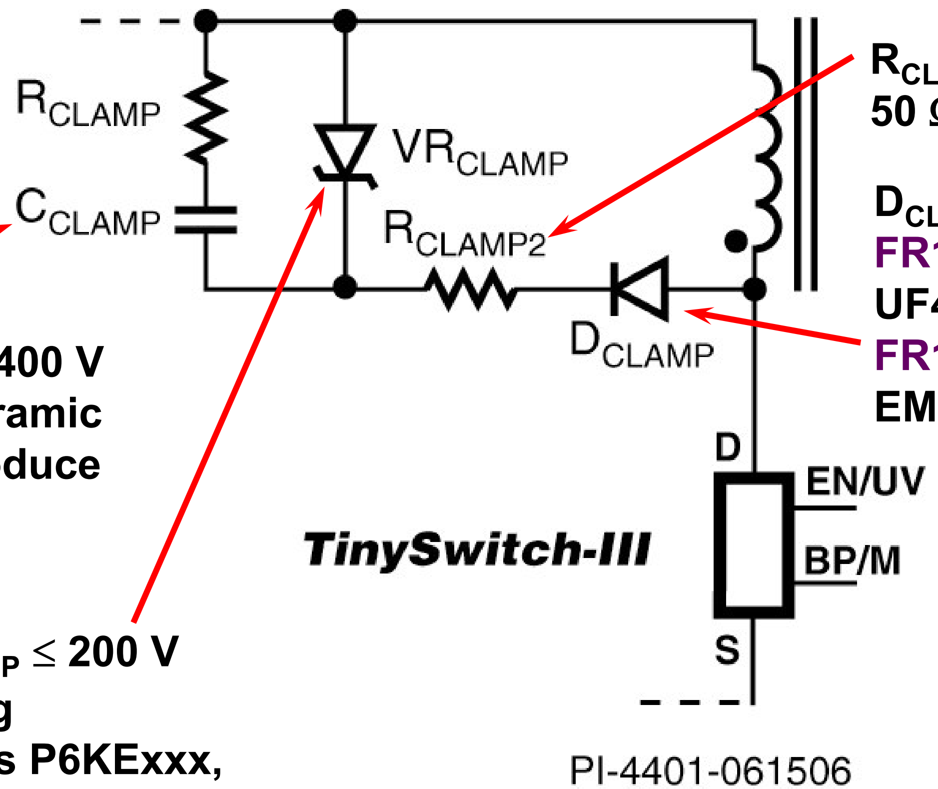
- **Improved efficiency and lower no-load consumption than RCD clamp**
- **Generates higher EMI than RCD clamp**
  - Placing R_{CLAMP3} (47 kΩ to 330 kΩ) in parallel with VR_{CLAMP} can reduce EMI and decrease zener dissipation
- **R_{CLAMP2} dampens ringing when a 500 ns diode (FR107) is used**

RCD/Zener Clamp Circuit

R_{CLAMP}:
47 kΩ to 200 kΩ,
½ W

C_{CLAMP}:
330 pF to 3.3 nF, ≥ 400 V ceramic or film (ceramic capacitors may produce audible noise)

VR_{CLAMP}:
$1.4 \times V_{OR} \leq VR_{CLAMP} \leq 200$ V
0.5 W to 1 W rating
Part number series P6KExxx, BZY97Cxxx, BZX55



R_{CLAMP2}:
50 Ω to 330 Ω, ¼ W

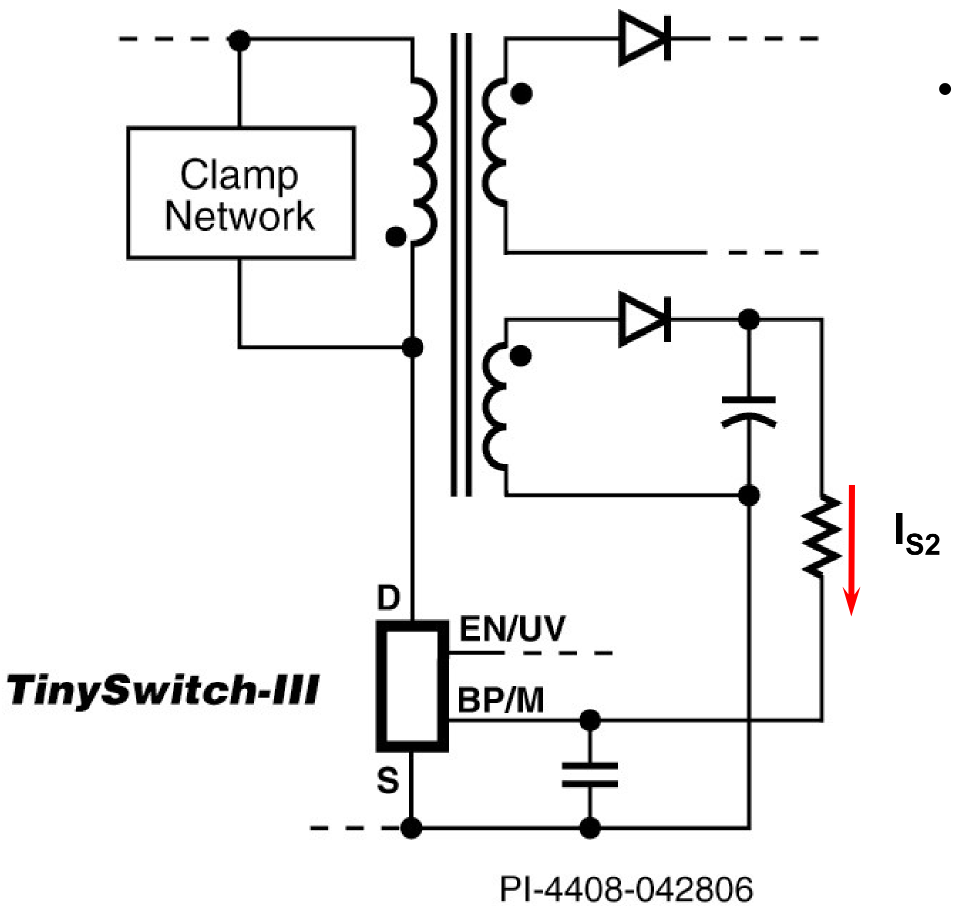
D_{CLAMP}:
FR107, 1N4937 or UF4005.
FR107 gives best EMI and efficiency

- **For applications where lowest no-load consumption, highest light load efficiency and low EMI are most important**

Combo RCD/Zener Clamp Design Guidelines

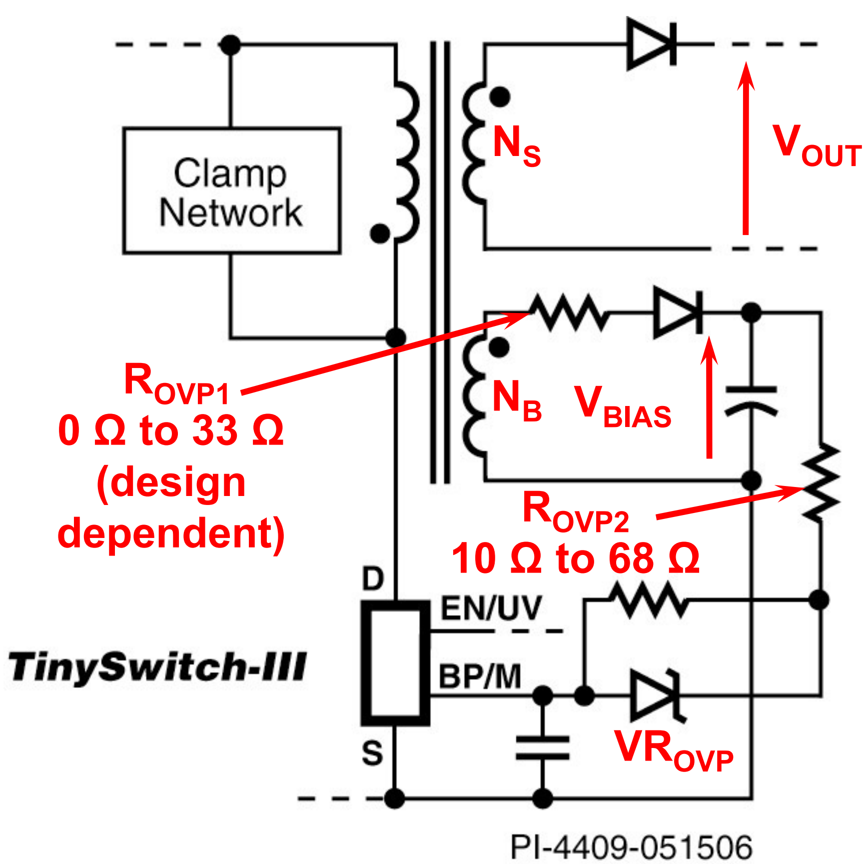
- **Highest efficiency and lowest no-load consumption clamp circuit**
- **Parallel capacitor softens Zener turn-on**
  - A 330 pF to 3.3 nF capacitor can lower EMI and increase efficiency
  - Allows low cost 1 W Zener (BZY97-C200) to be used in high power designs
- **R_{CLAMP2} dampens ringing and limits diode reverse recovery current**
- **Set initial value of R_{CLAMP2} at 200 Ω**
  - Adjust value for optimum EMI and efficiency
- **Fast diodes produce higher efficiency and lower EMI than ultra-fast**
  - Avoid general purpose rectifier diodes (1N400x) due to excessive ringing

Bias Winding Reduces No-Load Input Power



- **A bias winding reduces the no-load consumption to <50 mW**
  - IC supply current is no longer provided from the DRAIN pin
  - Select resistor value to provide the supply current (I_{S2}) specified in the *TinySwitch-III* datasheet
  - Internal clamp limits maximum BP/M pin voltage

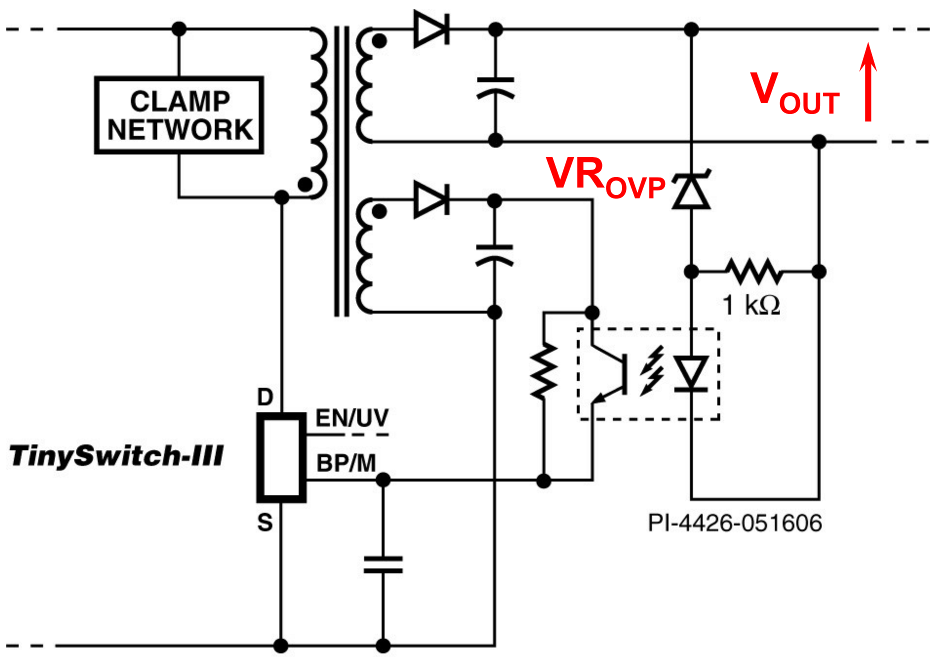
Primary Side Sensed OVP Guidelines



Primary Sensed OVP

- **$V_{BIAS} \approx (V_{OUT} \bullet N_B/N_S)$**
  - High bias voltage improves accuracy by reducing the effect of leakage inductance
  - 12 V to 22 V works well
- **Zener voltage**
  - $V_{VR(OVP)} > V_{BAIS} + 6.2\ V\ (V_{BP\_PIN})$
- **R_{OVP1} filters leakage spikes**
- **R_{OVP2} can be used to adjust trip point**
- **Verify that OVP does not falsely trigger**
  - Test at low line, maximum load where leakage energy is highest
  - Perform startup at highest line, zero load, where output overshoot is maximum
- **Monitor VR_{OVP} current to determine design margin to 6 mA threshold**

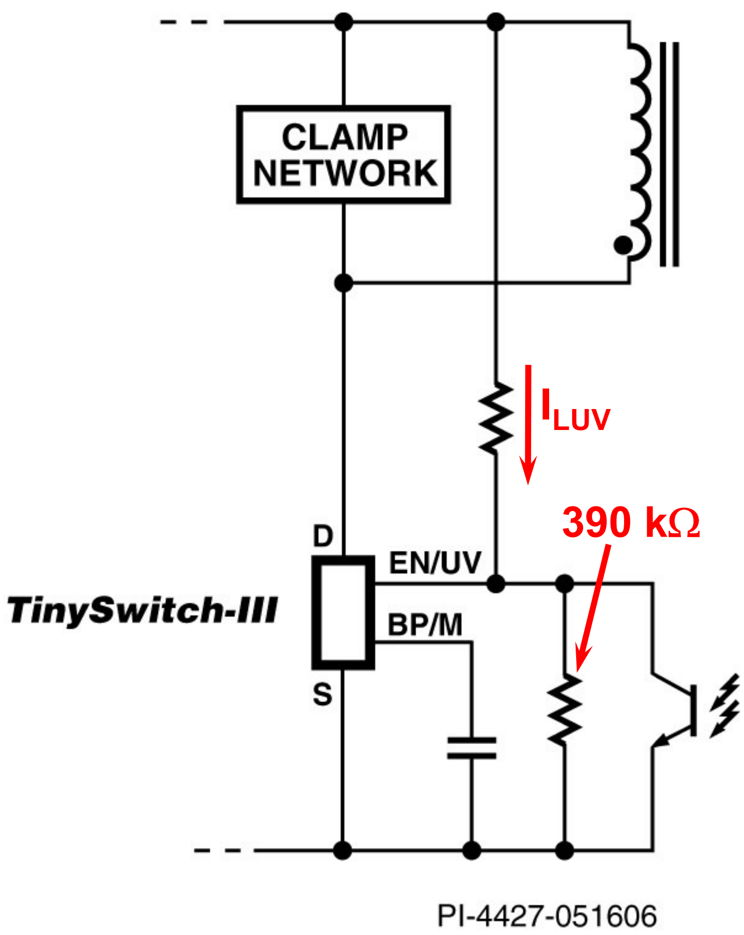
Secondary Side Sensed OVP Guidelines



Secondary Sensed OVP

- **Bias voltage: 12 V**
  - Insensitive to bias variation
- **Zener voltage:** **$V_{VR(OVP)} > V_{OUT(MAX)} + V_{F(OPTO)}$**
  - 1 kΩ resistor biases Zener close to test current for improved accuracy
- **OVP latch triggered when output voltage exceeds VR_{OVP} plus forward drop of opto LED**

Under-voltage Lock-Out (UVLO) Guidelines

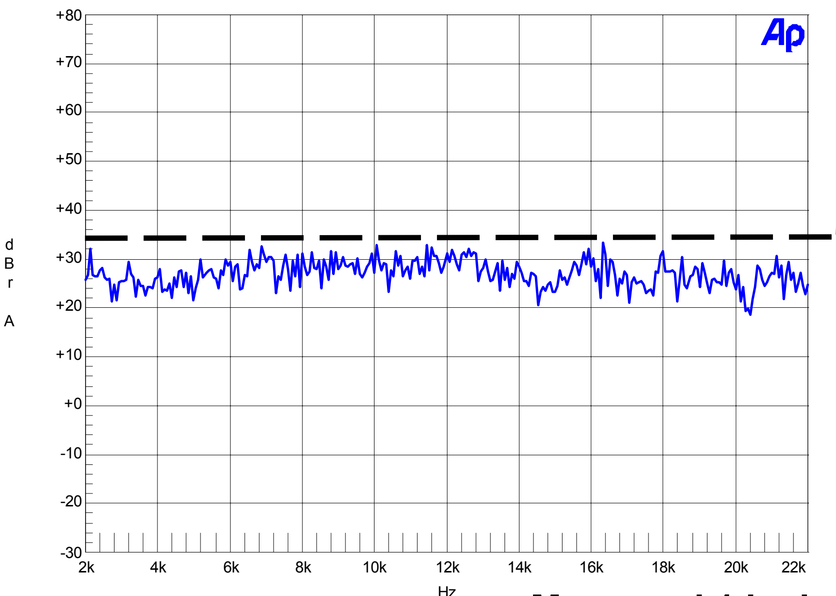


- **R_{UV} = (V_{UV}-V_{EN}) / 25 μA**
  - V_{EN} = 2.2 V at I_{EN} = 25 μA
  - V_{UV} is typically 100 VDC for universal input, 200 VDC for 230 VAC input designs
    - 3.9 MΩ for 100 VDC, 8.2 MΩ for 200 VDC
- **Voltage rating of >400 V required**
  - 0.5 W resistor or 2 series 0.25 W parts
    - Actual dissipation ≈35 mW
- **With no R_{UV} (I_{LUV} < 1 μA), UVLO is disabled**
  - Install a 390 kΩ resistor from the EN/UV pin to the SOURCE pin, in open frame designs
    - Prevents PCB leakage current from the BP/M pin to the EN/UV pin, which can cause false UVLO resistor detection and keep the power supply from starting up

Audible Noise Design Guidelines

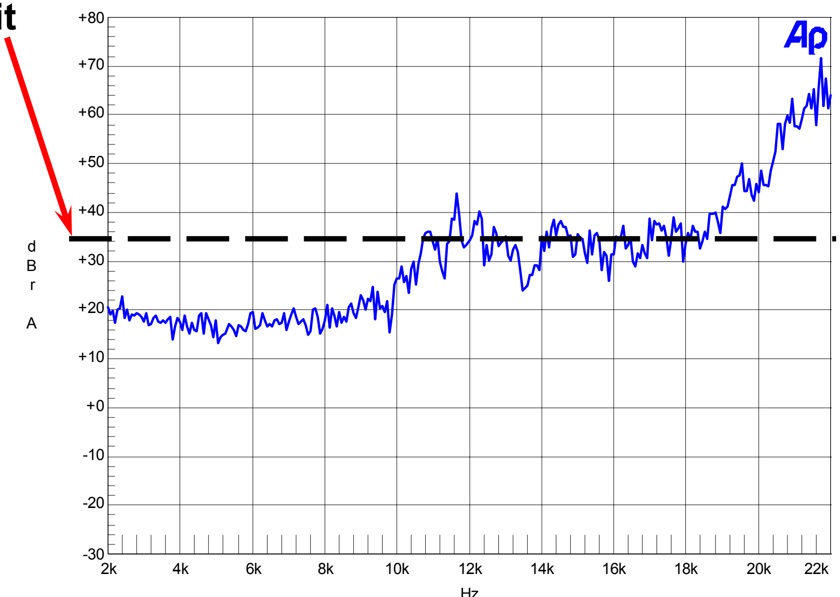
- **Flux density > 3000 Gauss may produce perceptible audible noise**
- **Long cores (EEL types) increase noise due to “tuning fork” effect**
  - Can be reduced by lowering flux density
- **35 dBA is the typical acceptable limit for audible noise**
  - Sealed enclosures attenuate audible noise by ≈10 dBA

3000 Gauss (300 mT) Short Core



35 dBA limit

3000 Gauss (300 mT) Long Core



Measured 1 inch (25 mm) from transformer

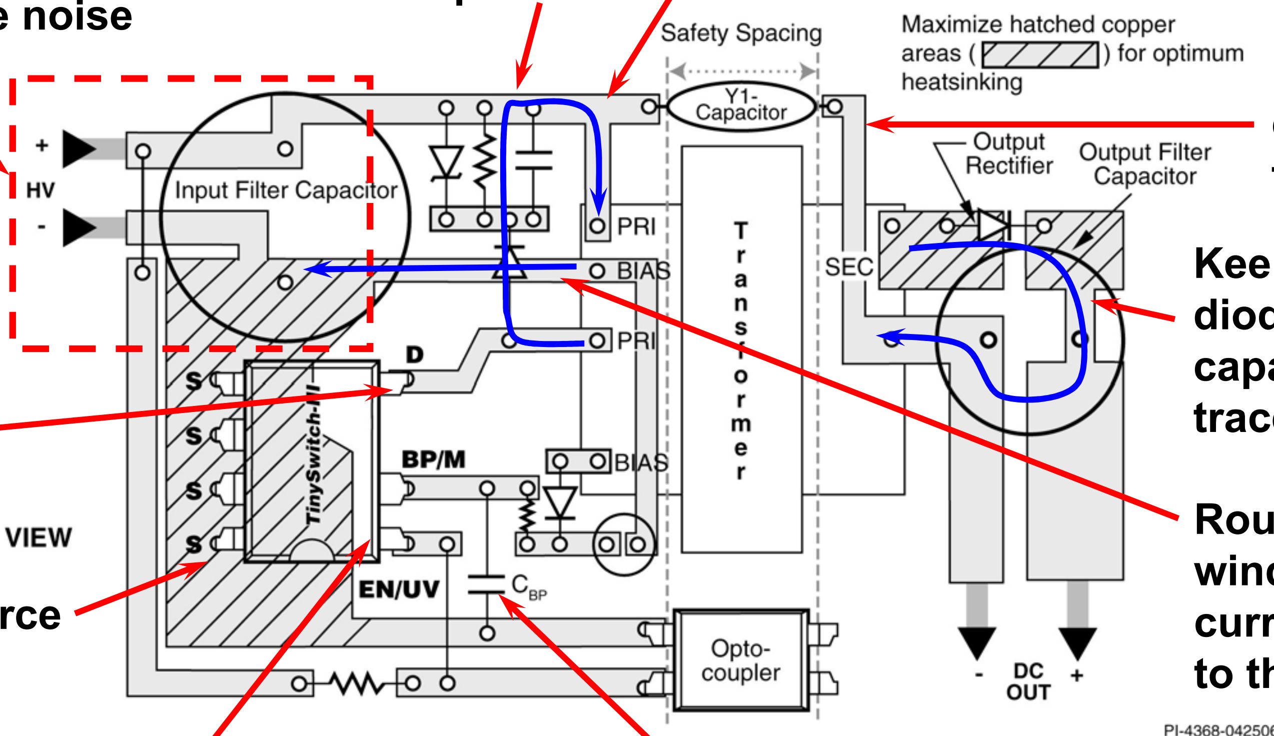
TinySwitch-III Layout Recommendations

Keep input stage away from IC DRAIN pin to minimize noise coupling

Keep clamp loop short

Connect Y capacitor to the plus bulk rail on the primary side for better surge immunity

Keep Y capacitor traces short



Keep output diode to output capacitor traces short

Keep drain trace short

Route bias winding currents back to the bulk cap

Maximize source area for good heatsinking

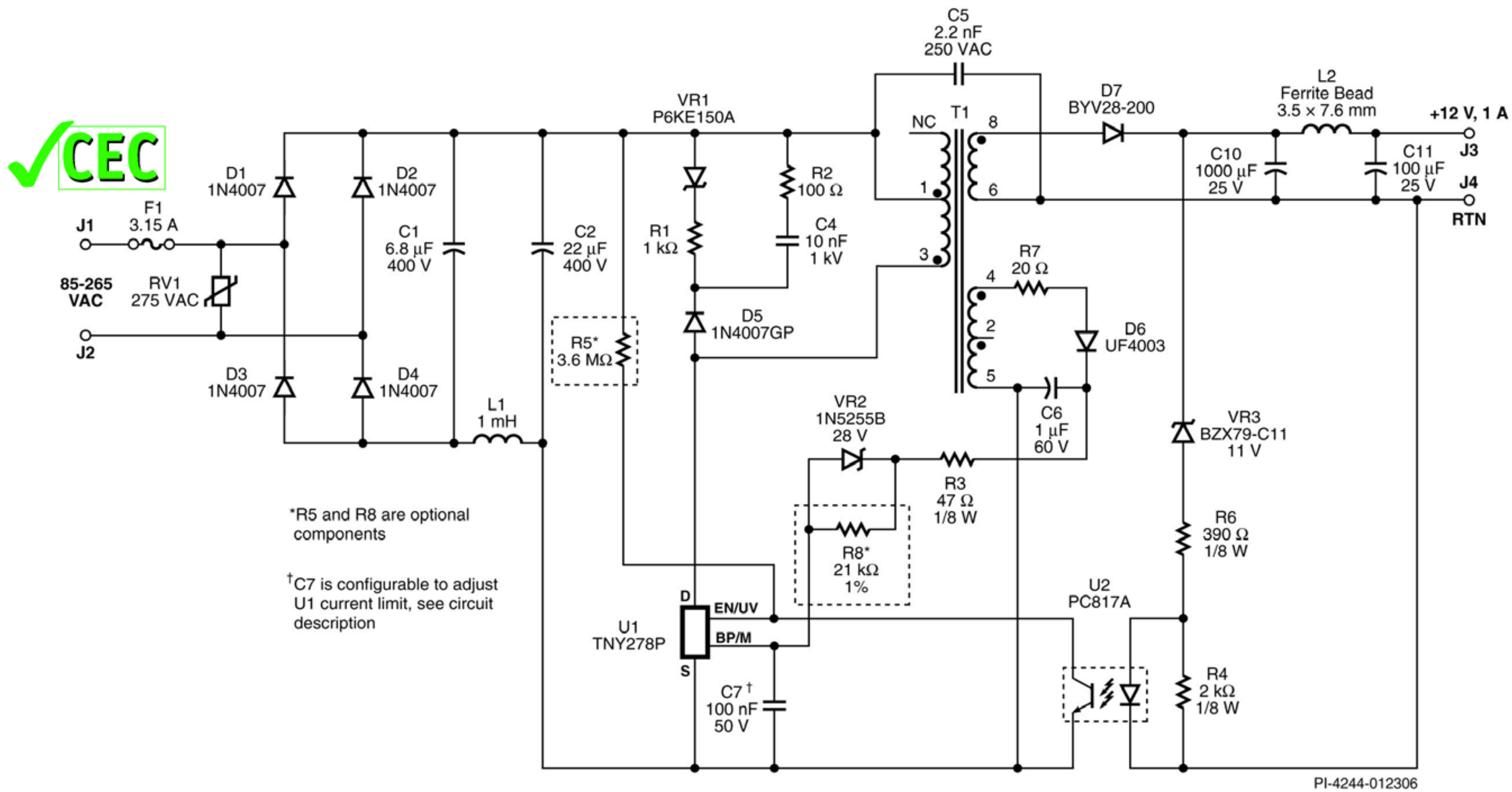
Keep traces above source potential away from EN/UV pin

Place BP pin capacitor near the IC

TinySwitch-III

Design Examples

EP91 – 12 V, 12 W Universal Input Supply



- **No-load with R8:** **< 50 mW**
- **No-load without R8:** **< 140 mW**
- **Average efficiency:** **> 80%**
- **Component count:** **33**

Available standby power @ 230 VAC
2.2 W for 3 W input power
1.4 W for 2 W input power
0.65 W for 1 W input power

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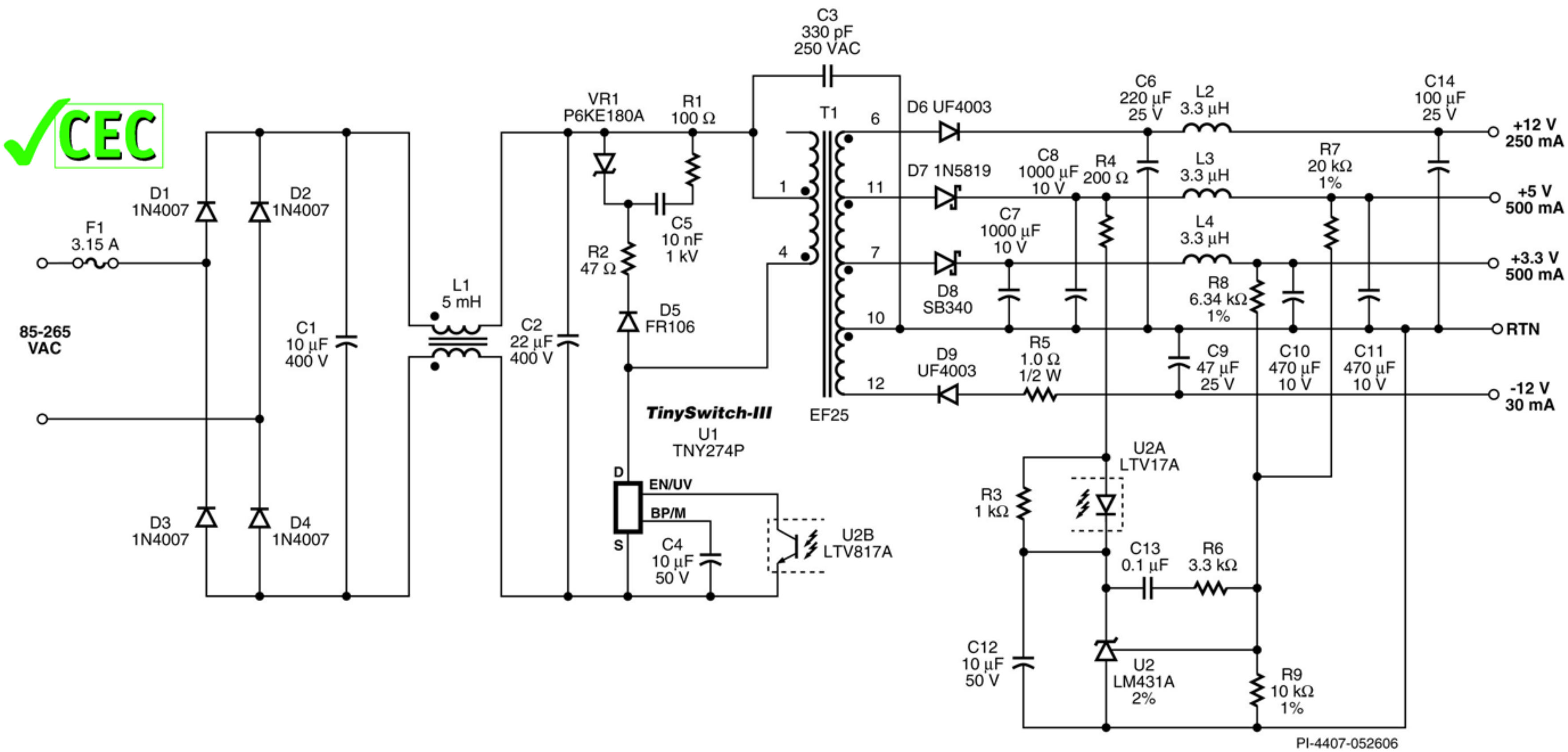
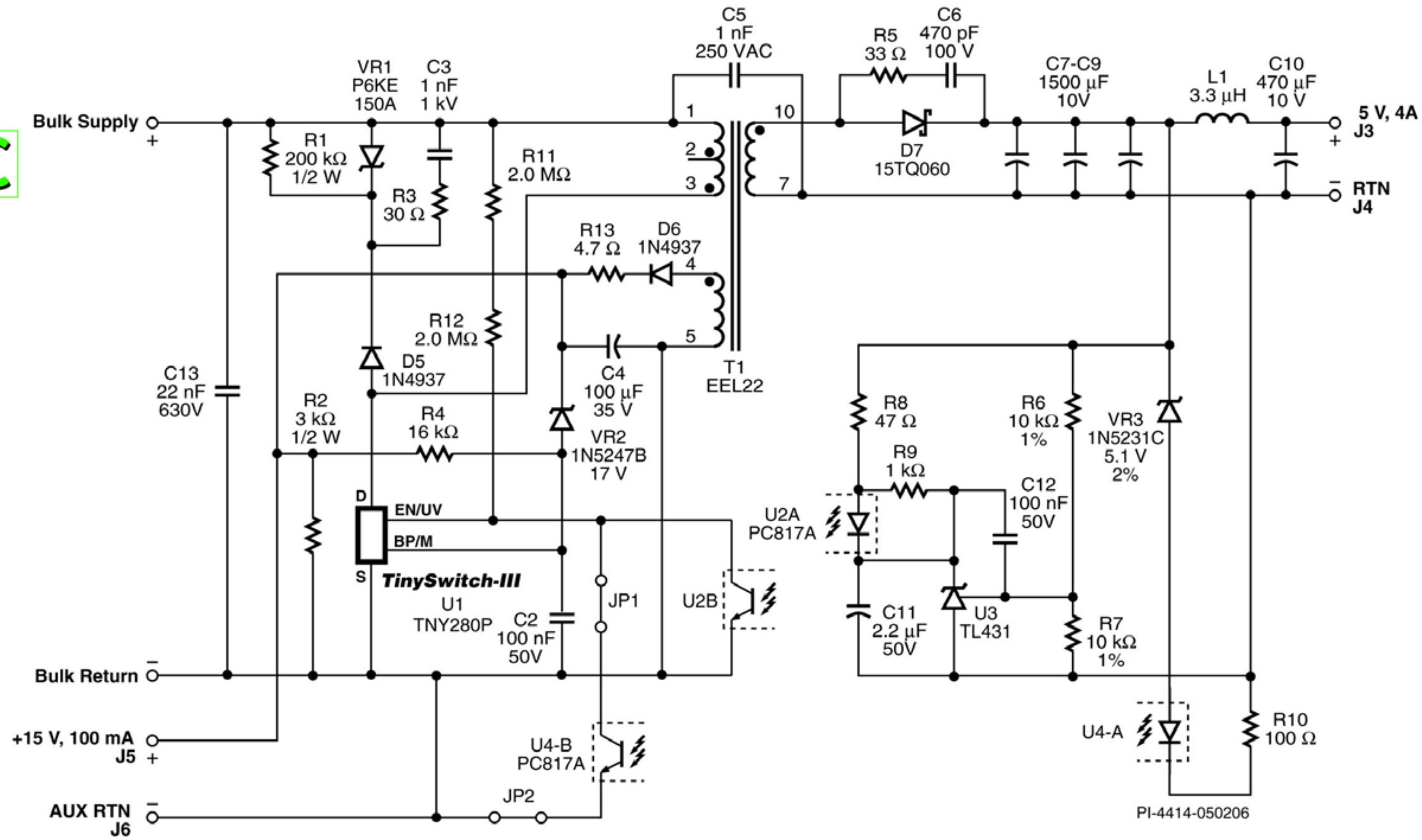
7.5 W Multiple Output (DVD) Supply



- **No-load consumption: <140 mW**
- **Average efficiency: >70 %**
- **Component count: 42**

Available standby power @ 230 VAC
2.1 W for 3 W input power
1.3 W for 2 W input power
0.6 W for 1 W input power

21 W Dual Output PC Standby Supply



- **No-load consumption: < 50 mW**
- **Average efficiency: > 80 %**
- **Component count: 42**

Available standby power @ 230 VAC
2.3 W for 3 W input power
1.48 W for 2 W input power
0.67 W for 1 W input power

PI Device Quick Design Checklist

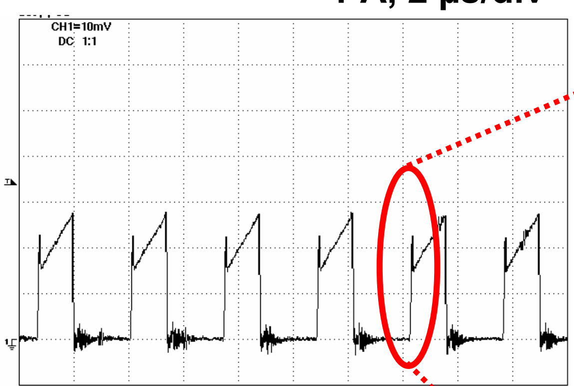
Quick Design Checklist

- **Maximum (peak) drain voltage**
  - V_{DS} should not exceed 650 V at $V_{IN(MAX)}$ and peak (overload) power
    - Provides 50 V margin to the 700 V BV_{DSS} rating
- **Maximum (peak) drain current**
  - Observe drain current waveforms for signs of transformer saturation at maximum ambient temperature, $V_{IN(MAX)}$ and peak (overload) power
  - Peak drain current must remain below the specified absolute maximum specifications under all operating conditions
- **Leading Edge Blanking**
  - Observe the leading-edge current spike on the drain current waveform and verify that it is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$

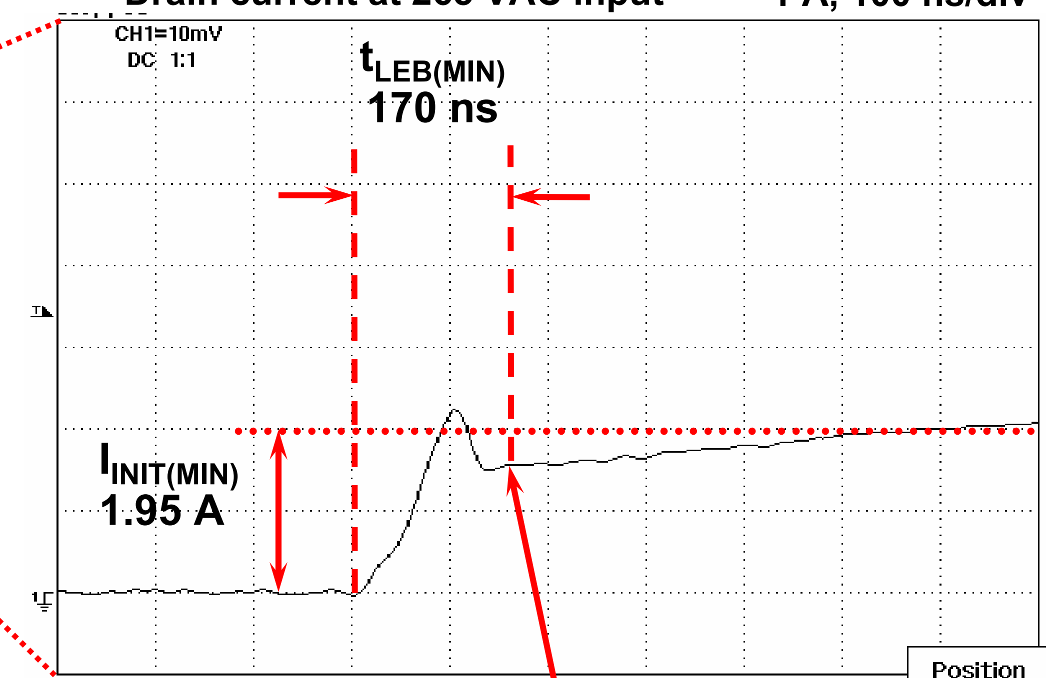
Leading Edge Blanking Verification

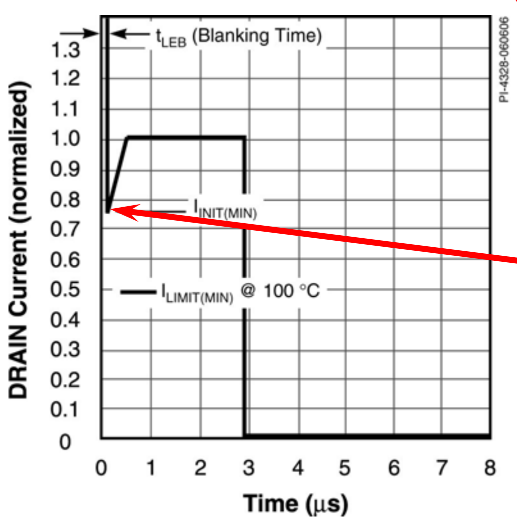
***PeakSwitch* datasheet specified minimum blanking time (t_{LEB}) = 170 ns**

1 A, 2 µs/div



Drain current at 265 VAC input **1 A, 100 ns/div**





$I_{INIT(MIN)}$ = 0.75 • $I_{LIMIT(MIN)}$

Drain current well below $I_{INIT(MIN)}$ after $t_{LEB(MIN)}$

External Power Supply (EPS) Energy Efficiency Standards

Appendix A

The Problem of Energy Waste

- **Energy waste is a major concern around the world**
  - Fossil fuel energy sources are finite
  - Fossil fuel consumption side effects: pollution, green-house gases
  - Energy costs are increasing, while alternative energy sources are not mature enough to provide relief
- **The growing demand for personal electronics has dramatically increased the number of External Power Supplies (EPS)**
- **How much energy do EPS actually consume each year?**

The Magnitude of Energy Waste

Estimated EPS sold annually:	**>1 billion units**
Estimated EPS currently in use:	**>10 billion units**
% of EPS that are inefficient linears:	**~ 45%**
Yearly EPS energy waste in the US:	**30 – 60 B kW-hours**
Cost of annual US EPS waste :	**2.5 – 5 billion dollars**

Although EPS waste is only 1-2% of annual US energy consumption, it equals the output of 26 average sized power plants!

Regulations Emerge to Reduce Energy Waste

Regulation Name Description	***Geographic Region Affected***	***Effective Date***	***Compliance Required***
ENERGY STAR	United States	January 2005	voluntary
EU Code of Conduct	Europe	January 2007*	voluntary
China Certification Center for Energy Conservation Products (CECP)	Mainland China	January 2005	voluntary
California Appliance Efficiency Regulations (Title 20)	California	January 2007**	mandatory
Australia Greenhouse Office (AGO)	Australia	October 2007	mandatory
HB 3363	Oregon	January 2007	mandatory
Energy and Consumer Savings Act	Rhode Island	January 2007	mandatory
SB 6840	Washington	January 2008	mandatory
HB 2390	Arizona	January 2008	mandatory

*Standards have been in effect since 2001. In January 2007, it plans to harmonize EPS active-mode efficiency standard with the others shown. ** Additional products covered in July 2007.

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CALIFORNIA CODE OF REGULATIONS, TITLE 20, SECTIONS 1601 - 1608

Standards for [External] Power Supplies Effective January 1, 2007

Nameplate Output (W)	*Minimum Efficiency in Active Mode*
< 1 Watt	0.**49** * Nameplate Output
≥ 1 (W) ≤ **49** Watts	(0.09 * Ln(Nameplate output)) + 0.**49**
> **49** Watts	0.**84**
	Maximum Energy Consumption in No-Load Mode
0 to < 10 Watts	0.50 Watts
≥ 10 to < 250 Watts	0.75 Watts
Where Ln (Nameplate output) = Natural Logarithm of the output power in Watts	

Note: Active-mode efficiency is the average of the 25%, 50%, 75%, and 100% load points
In 2008, the minimum active-mode efficiency for EPS > 51 watts will be 0.85,
and the maximum no-load consumption for all EPS < 250 watts will be 0.5 watts

Additional Energy Efficiency Programs

- US 1W Standby Executive Order
- Japan Top Runner Program
- Korea Energy Saving Office Equipment & Home Electronics Program
- Germany Blue Angel
- US Ecos Consulting 80-Plus Program
- European Group for Energy Efficient Appliances
- EU Directive 2005-32-EC (EuP Directive)

Meeting Worldwide Requirements

- **PI solutions enable conformance to ALL worldwide energy efficiency standards including standards with tighter no-load consumption limits**
  - European Union Code of Conduct requires < 300 mW
  - Some Japanese and European OEMs require < 150 mW
  - Other Japanese OEMs require < 50 mW

Stay Informed with PI's Green Room

- **The PI Green Room contains information and links to the latest worldwide standards**
  - www.powerint.com/greenroom
  - View regulations and standards for your design:
    - By agency (ENERGY STAR, CEC, CECP, AGO, etc.)
    - By application (external adapter/charger, TV, DVD player, etc.)
    - By region (China, Asia, Europe, US, etc.)

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Links to Key Documents

- Current version of the CEC Appliance Efficiency Regulations
  http://www.energy.ca.gov/appliances/
- US EPA ENERGY STAR power supply efficiency specification
  http://www.energystar.gov/index.cfm?c=prod_development.power_supplies
- US EPA test method for calculating the efficiency of single voltage external AC-DC and AC-AC power supplies
  http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf
- EU Code of Conduct external power supply efficiency web page
  http://energyefficiency.jrc.cec.eu.int/html/standby_initiative_External%20Power%20Supplies.htm