

PRELIMINARY DATA SHEET

MARCH 2006

GENERAL DESCRIPTION

The Teridian 78Q8430 is a single chip 10Base-T / 100Base-TX capable Fast Ethernet Media Access Controller (MAC) and Physical Layer (PHY) transceiver. The device is designed specifically for the Audio/Visual (A/V) and Set Top Box (STB) markets and is easily interfaced to available A/V and STB core processors.

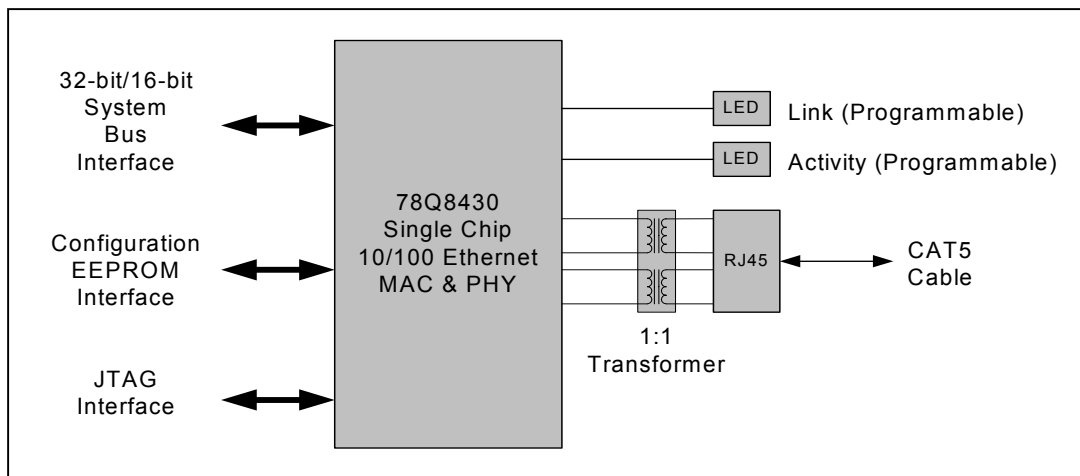
The 78Q8430's integrated transceiver includes scrambler/descrambler, dual speed clock recovery, and full-featured auto-negotiation functions. The transmitter includes on-chip pulse-shaper and a low-power line driver. The receiver has an adaptive equalizer and a baseline restoration circuit required for accurate clock and data recovery. The Ethernet transceiver is connected to the cable via 1:1 isolation transformers. No external filter is required. The 78Q8430 operates over Category-5 Unshielded Twisted Pair (CAT-5 UTP) cabling in 100Base-TX applications and can operate over CAT-3 UTP in 10Base-T applications.

The 78Q8430 is compliant with applicable IEEE-802.3 standards. MAC and PHY configuration and status registers are provided as specified by IEEE802.3u. The integrated MAC is supported by an internal 32K Byte transmit and receive SRAM. The partition of transmit and receive FIFOs are configurable through software, allowing the 78Q8430 to be tuned for specific applications. A host processor may interface directly to these FIFOs via the 32-bit bus interface. The bus can also be configured for 16-bit or 8-bit bus widths. The device contains hardware support for TCP-IP checksum. It generates the checksum for transmitted packets, and calculates and verifies the checksum for received packets. Complete, portable device drivers are available for OS20, Linux and VxWorks.

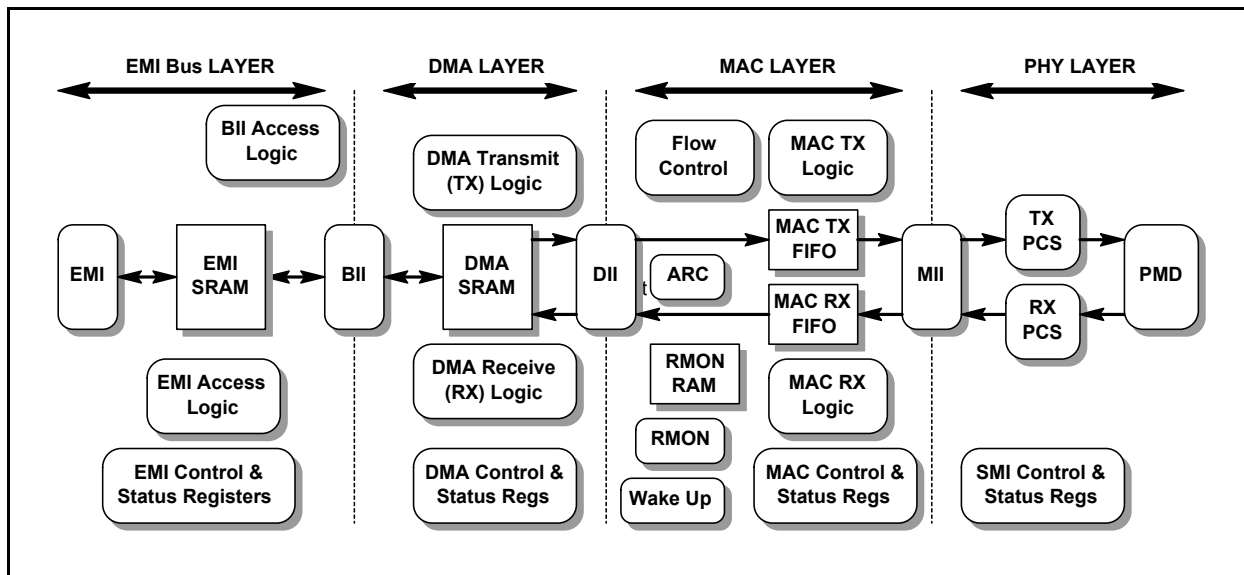
The 78Q8430 is designed for high performance and low power operation, and operates from a single 3.3V supply. Power down modes and power saving modes are available. Wake up events such as Magic Packet™, OnNow Pattern and External wake-up are also supported.

FEATURES

- Single chip 10Base-T / 100Base-TX IEEE-802.3 compliant MAC and PHY, requiring only a dual 1:1 isolation transformer interface to the line
- Full Auto-Negotiation capable
- Auto-Polarity detection and correction
- Auto-MDIX to correct non-crossover cables
- System bus interface mimics SRAM: configurable for 32b, 16b or 8b data widths (big end-in and little end-in operation available for 32b data, little end-in operation for 16b data)
- Optional internal 100 MHz BUSCLK generation enabling asynchronous bus operation without system provided bus clock
- Extremely deep Tx and Rx FIFO (32KB total) – partition is configurable via software
- On-chip 21 address perfect match ARC
- On-chip TCP and UDP protocol checksum generation, calculation and verification
- Support for IEEE802.3x flow control
- Supports VLAN
- Remote Management (RMON)
- SNMP management protocol
- Full duplex operation capable
- 2 Programmable PHY status LED indicators
- Secondary MII interface available for expansion to 100Base-FX, HPNA2.0 PHYs or other 802.3 based networking technologies
- Low Power
 - Single 3.3V supply @ 450 mW
 - Power-saving and power-down modes
 - Supports wake up events including Magic Packet™, OnNow Pattern Matching and External Event monitoring.
- 128-pin LQFP Package
- Built in boundary scan self test



78Q8430 System Interface Diagram



78Q8430 Device Block Diagram

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1 FUNCTIONAL DESCRIPTION

1.1 Introduction

The 78Q8430 is an Ethernet controller suitable for use in Set-top Box and other embedded applications. This document specifies support for an External Memory Interface (EMI) connection to ST-20 based micro-processors, such as the STi5514 or STi5516B. The 78Q8430 operates at network data rates of 100-Mbit/sec or 10-Mbit/sec and includes support for Magic Packet®, OnNow®, and the Advanced Configuration and Power Interface (ACPI) Specification. The controller features an integrated 10BASE-T and 100BASE-TX PHY, which provides a minimum chip solution for Ethernet or Fast Ethernet over twisted pair connections. This transceiver complies with the IEEE 802.3-2000 standard for 10-Mbps and 100-Mbps operation, and includes support for automatic MDI/MDI-X cross-over configuration, making cabling easy in the consumer environment.

The controller supports connection via the EMI port as an external SRAM device, with timer delayed interrupts to assist in managing network and system data flow. The Ethernet Controller is accessed as an SRAM device by the ST-20 processor for reading and writing control and status registers, accessing network statistics, and moving data. The EMI bus can be configured as either 32-bits, 16-bits, or 8-bits. The ST-20 or general purpose DMA (GPDMA) moves the data to and from the Ethernet Controller with simple SRAM accesses of 4-bytes, 2-bytes, or 1-byte, depending on the bus width.

The 78Q8430 does not have DMA request and acknowledge control pins for interfacing with an external DMA controller. Burst mode and automatic address generation are not supported by the 78Q8430. The CPU or system DMA controller must generate a CSB cycle with proper device address for each bus transaction.

The EMI-based Ethernet controller features an integrated memory block with a SRAM interface. When combined with the integrated 10/100 PHY circuit, this provides a minimum component solution for a complete Ethernet subsystem. By supporting both 100- and 10-Mbit/s speeds, new products may be deployed into markets which are in transition. The 78Q8430 Ethernet controller operates in either Full Duplex or Half Duplex mode with the integrated transceiver. In full duplex mode, the controller implements the IEEE 802.3 MAC Control Layer and the PAUSE Operation for flow control. The controller support for PAUSE Operation includes programmable support for additional MAC Control functions. In half duplex mode, the controller implements the IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol.

The controller features a network management block which maintains onchip hardware counters for RMON, SNMP, and other popular network management protocols. This off-loads the processor from maintaining network statistics needed for managed Ethernet applications.

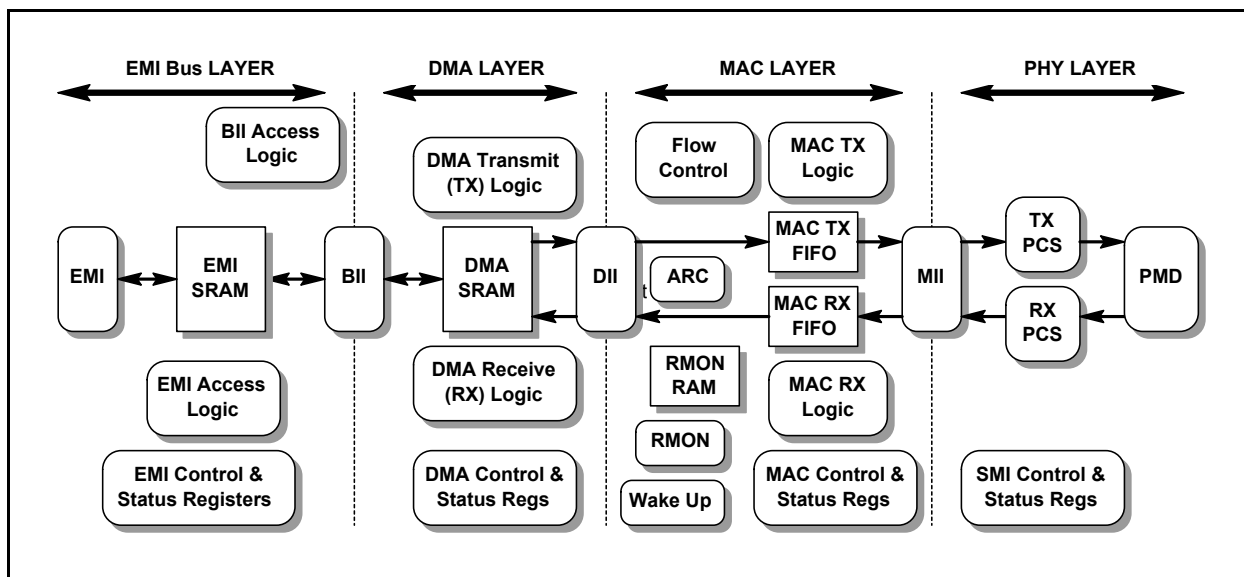
The controller supports alignment control for received packets to facilitate alignment for processing by software.

1.2 Overview

The 78Q8430 is divided into four sections.

- EMI Bus Control Layer
- Internal Direct Memory Access (DMA) Layer
- Ethernet Media Access Control (MAC) Layer
- Ethernet Physical (PHY) Layer

Figure 1 : Device Block Diagram



Teridian Semiconductor Ethernet designs make use of three standard interfaces between the four layers:

- Between the PHY and MAC layers, the 78Q8430 supports the Media Independent Interface (MII). The MII is part of the ISO approved IEEE 802.3 100BASE-T standard for 100 Mb/s Ethernet. It supports either full or half duplex operation, and transfers 4-bits of data at 25 MHz or 2.5 MHz.
- Between the MAC and DMA layer, there is a simple byte-wide hand-shake protocol, called the DMA Independent Interface (DII).
- Between the DMA layer and the Bus layer, there is a Bus Independent Interface (BII).

The EMI Bus Layer includes on-chip SRAM blocks to store packets prepared for transmission and packets received over the Ethernet connection. The EMI supports data transfers at up to 100 MHz, depending on the processor choice. Data is transferred to and from the EMI bus by either a GPDMA module or the ST-20. For register read and write operations, a bus address decoder in the EMI interface block supports access to EMI, DMA, and MAC Control and Status Registers.

The DMA Layer provides separate Transmit (Tx) and Receive (Rx) logic blocks. These blocks define the memory data structures and access rules for software drivers. By separating the bus interface from the DMA engine, software drivers can be easily ported from one processor and bus configuration to another. The DMA layer includes an on-chip single ported Static RAM (SRAM) block. This block is used to store transmit and receive data, addresses for the Address Recognition Circuit (ARC), and control information for multiple packets.

The MAC layer consists of transmit and receive logic blocks, a flow control block, an Address Recognition Circuit (ARC), and two small dual-port FIFO buffers. The MAC FIFO buffers provide some DMA latency and are used to synchronize data between the network and system clock domains. In addition, the transmit FIFO supports retransmission after collision without backing up the DMA engine.

The MAC layer has hardware support for standard Ethernet statistics. The block supports RMON, SNMP, and Internet standards for managing networks. The block contains logic and small SRAM blocks to ensure that all statistics can be maintained while transmitting or receiving small back-to-back packets at full line bandwidth.

As an extension to the MAC layer, the controller includes an Address Recognition Circuit (ARC). This circuit provides address matching and packet type filtering services which are part of the Link Layer functions. By using the ARC, software drivers can off-load much of the work of packet filtering, reducing the processing load on the CPU.

1.2.1 Application Environments

Figure 2 shows a simple application diagram for a design using the EMI-based 100/10-Mbit/s Ethernet Controller. By providing a direct connection to the EMI bus, applications requiring Ethernet network access can be realized with a high degree of integration. The figure shows the STi5514 or similar processor and the Ethernet controller with connected Address and Data buses. This connection can be either on the mother board, or via a STEM expansion module. The EMI Controller of the STi5514 controls the address and data and the other control signals.

Figure 2 : System Block Diagram

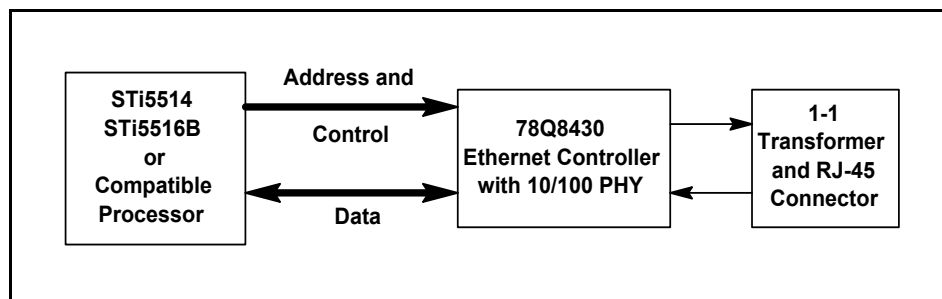
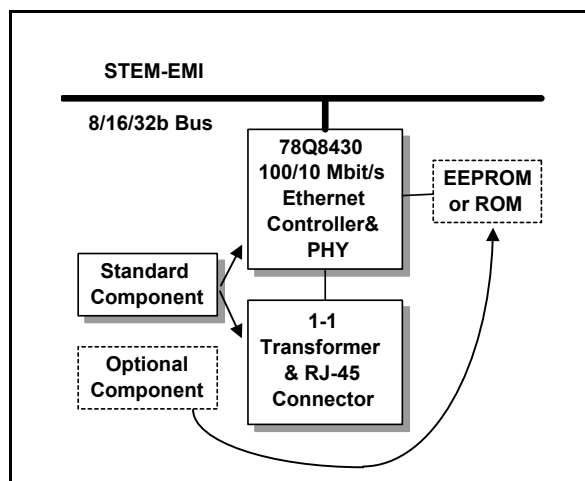


Figure 3 shows the components that are likely to be used with the 100/10-Mbit/s Ethernet Controller. The integrated PHY is designed to be directly connected to an integrated 1-1 transformer and RJ-45 connector, in order to provide a minimum parts solution.

Figure 3 : EMI Bus Diagram



The system designer has an additional option: An optional serial programmable ROM or EEPROM can provide the controller with its Ethernet station address upon power-up. This option is not needed if the system has an alternate way to provide a unique Ethernet address.

1.2.2 Supply Voltages

The 78Q8430 requires a single 3.3 V (+/-0.3 V) supply voltage. No external components are required to generate on-chip bias voltages and currents. High accuracy is maintained through a closed-loop trimmed biasing network. On chip power converters generate 1.8 V power for core digital logic and memory blocks. The voltage regulator is not affected by the power-down mode.

1.2.3 Operating Modes and Power Management

The 78Q8430 supports several operating and test modes.

- ❑ Normal Mode: both the Controller and PHY are active.
- ❑ MAC MII Mode: the Controller is active, but the PHY is powered down. The MAC communicates via an exposed MII to a external PHY, such as HomePNA or fibre optic.
- ❑ Scan Test Mode: This mode is used for manufacturing testing of digital logic.

The operating modes are controlled by the MAC_MII and PHY_TEST pins. When the PHY is active, it can be configured for normal operation or three power saving modes. When the EMI bus is active, it can be in normal mode or Power Management low power mode.

1.3 Feature and Benefit Summary

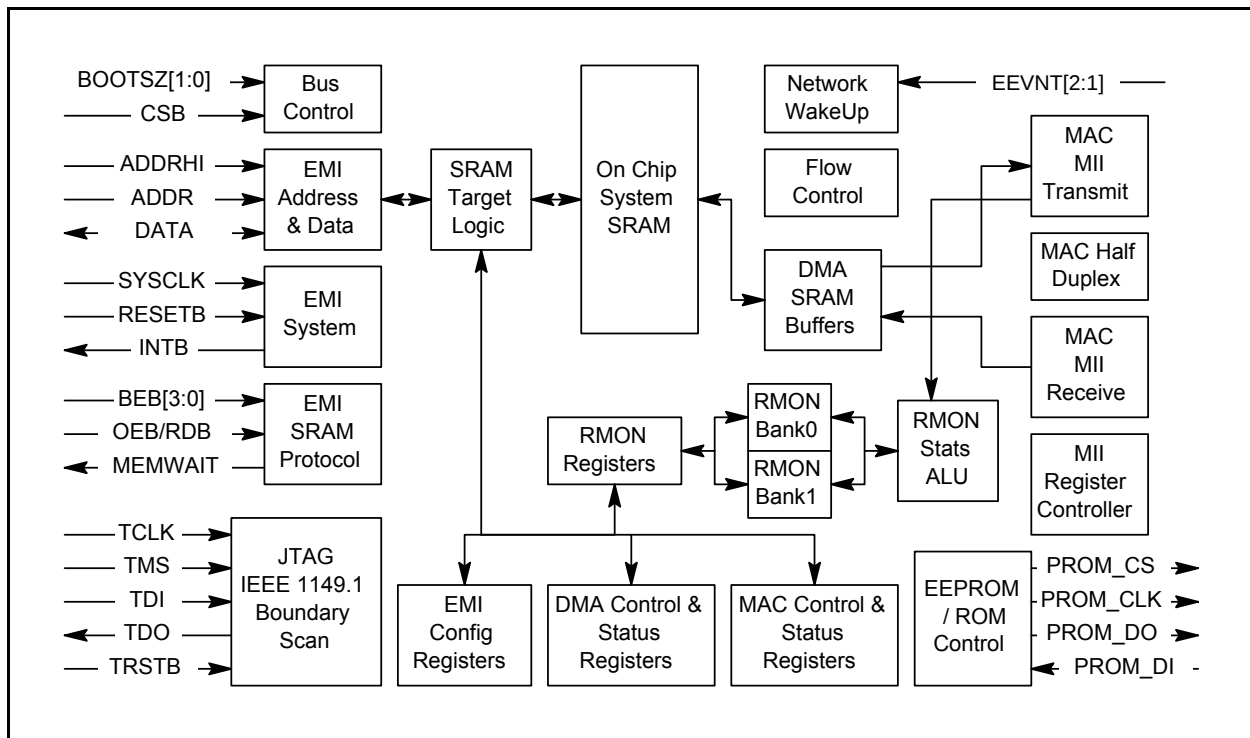
Table 1 : Feature and Benefit Summary

Feature	Benefit
EMI bus interface	Direct connection to ST-20 processors
Optional 100 MHz BUSCLK Generation	Asynchronous bus operation without system clock
On-chip SRAM block	No need for EMI memory chip
Integrated 10/100 PHY	Support minimum parts, low cost solutions.
ACPI Power Management	Supports standard power management S/W
Magic Packet®	Supports standard remote wake up
OnNow Wake Up	Maintain network connections while sleeping
Power Saving Modes	Supports low power applications
Receive Data Alignment	Align data for other processing requirements
Host not responding	Alert network: interrupts are not acknowledged
Event monitoring	Support remote security features
Network management H/W counters	Support RMON, SNMP, and network statistics.
Interrupt on link status and PHY events.	Active system monitoring of network links
16-bit and 8-bit bus modes	Cost effective solution for narrow bus CPUs
IP and TCP/UDP checksum generation	Off load CPU for protocol stack processing
Large DMA Transmit FIFO	Support for Jumbo packets with checksum generation.
16-Byte MAC receive FIFO buffer	Allow DMA Latency during system SRAM access
80-Byte MAC transmit FIFO buffer	Retransmit after collision without DMA action
Data alignment logic	Full data alignment freedom; high bus utilization
100/10-Mbit/s operation	Range of price/performance points. Phased conversion
Full IEEE 802.3 compliance	Compliant with existing applications software
VLAN support	H/W support for VLAN tagged packets
Auto-negotiation	Automatic link configuration
MDI/MDI-X automatic cross-over	Can use standard or cross-over cables.
PHY base line wander correction.	Reliable recovery of clock and data.
PHY adaptive equalization.	Reliable recovery of clock and data.
PHY polarity correction.	Automatic / manual setting of polarity reversal.
PHY power management	Low power requirements for normal operation.
Address recognition circuit	Filter network traffic, reduce CPU load
Optional ROM or EEPROM	Provides network address and configuration information
Full duplex mode	Doubles bandwidth
PAUSE operation	H/W support for full duplex flow control
Flexible MAC Control support	H/W support for future MAC Control Operations
Long packet mode	Support specialized environments
Short packet mode	Support specialized environments. Fast testing
PAD generation	Ease of processing. Reduced processing time
Transmit polling mode	Minimize system overhead to initiate transmission
Transmit wake-up control	Minimize system latency to transmission initiation
Receive early-notify control	Minimize system latency to processing received packet

1.4 Internal Block Diagrams

1.4.1 Internal BII, DII, and MAC

Figure 4 : Internal BII, DII, and MAC Block Diagram



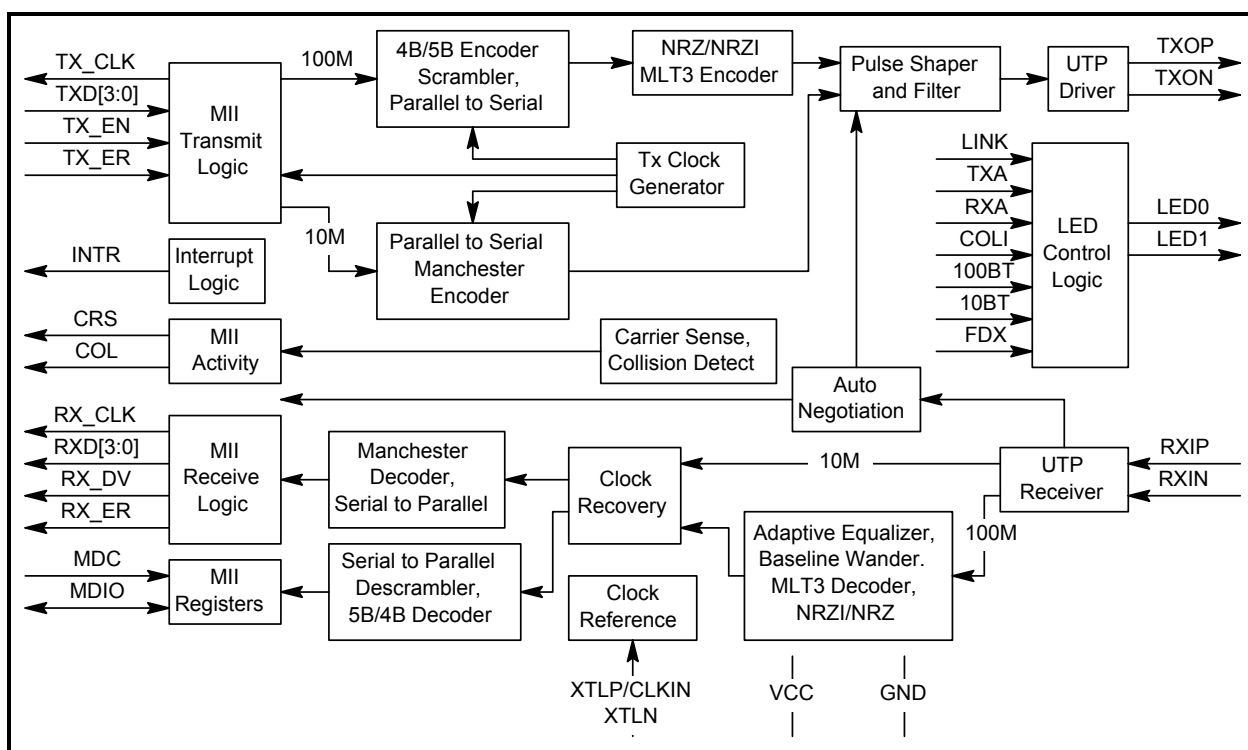
On the left side are the signals which connect to the EMI bus. On the upper and middle right, the blocks which implement the MAC side of the MII are shown. These blocks are connected to the embedded PHY. On the lower right, connections to the EEPROM/ROM are shown.

1.4.2 Internal PHY

Figure 4 gave a brief overview of the functional layers of the 78Q8430. This section shows the functional blocks in more detail, including the I/O signals.

Figure 5 shows the functional blocks of the internal 78Q8430 PHY. The signals shown on the left side are the internal MII signals to the MAC. These signals are multiplexed with their respective external pins for use with an external PHY device. The 78Q8430 is not a two port device. Only one PHY interface can be operational.

Figure 5 : Internal PHY Block Diagram



On the right side are the signals which connect to the status LEDs and a 1:1 isolation transformer before connecting to an RJ-45 connector, or equivalent media components.

1.5 EMI and DMA Functions

Figure 4 shows some of the functional blocks for configuring and controlling the EMI bus, and for transferring data to and from the DMA FIFO's:

- ❑ The EMI signals provide for address and data, EMI SRAM protocols, and system signals and controls.
- ❑ The EMI Configuration Registers provide for setup and control of EMI functions.
- ❑ The DMA Control and Status Registers allow setup and control of DMA operation.
- ❑ The Bus Master Controller provides for transfer of network data and data control structures.
- ❑ The Target Controller supports register read/write operations.
- ❑ The DMA SRAM provides for up to 8K bytes of on chip storage for data and packet controls.

There are two FIFO buffers controlled by the DMA engine. The DMA Transmit FIFO holds data and status information for packets being transmitted. The DMA Receive FIFO holds data and status information for packets being received. Each FIFO has a Producer control block, which controls data being placed in the FIFO, and a Consumer control block, which controls data being taken from the FIFO. In addition, part of the FIFO SRAM is set aside for control information, such as addresses to use for filtering in-coming packets, wake up data, and other control values.

The DMA control blocks provide logic for initiating bus master read and write operations across the EMI bus. They include:

- ❑ Bus size control.
- ❑ Transmit threshold control, to match transmission latency to EMI bus latency.
- ❑ Big-endian byte swapping, to support data transfers to big-endian processors.
- ❑ Buffer spanning and packing controls.
- ❑ Polling controls, to optionally poll for packets to transmit.
- ❑ Transmit Wake Up controls, to start transmission as soon as data is ready.
- ❑ Early notification, to allow processing of incoming data to begin before reception ends.
- ❑ Interrupt enable controls, to adjust controller behavior to protocol requirements.

1.5.1 Big Endian and Little Endian Byte Ordering

The EMI Bus defaults to a little endian bus, because the ST-20 is a little endian processor. However, network protocols tend to have Big Endian byte ordering, due to the historic role played by Big Endian processors in the early days of networking.

The 78Q8430 defaults to the natural little endian byte ordering, as shown in the following table.

Table 2: Byte Enables for little endian byte ordering

BYTE 3 (MSB)								BYTE 2								BYTE 1								BYTE 0 (LSB)							
BEB[3]								BEB[2]								BEB[1]								BEB[0]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The 78Q8430 also supports 32-bit Big Endian byte ordering, for data transferred to and from buffers under buffer descriptor control, as shown in the following table.

Table 3 : Byte Enables for big endian byte ordering

BYTE 0 (MSB)								BYTE 1								BYTE 2								BYTE 3 (LSB)							
BEB[3]								BEB[2]								BEB[1]								BEB[0]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note that while the bytes are reversed in order, the byte enables still control the same bits of the bus. No byte reversal is supported for data structures or slave mode register read/write. Only transfers of data buffers are affected by Big/little endian selection. The 78Q8430 does not support 16-bit Big Endian byte ordering when operating in 16-bit mode. For 8-bit mode, there is no difference between Big and little endian.

1.5.2 DMA Transmit Controller

The internal DMA transmit controller consists of two state machines: a producer and a consumer. The DMA transmit producer reads the transmit queue frame descriptor, and controls the transfer of data from the transmit queue to the transmit data FIFO. It also controls the writing of transmit status information, which gives MAC status information about transmitted packets, after transmission is complete. The DMA transmit consumer controls the MAC transmit engine and the movement of data from the DMA transmit FIFO to the smaller MAC transmit FIFO. The DMA transmit controller controls the generation of interrupts for transmitted packets after the transmit status information has been written to system memory.

1.5.3 DMA Receive Controller

The internal DMA receive controller consists of two state machines: a producer and a consumer. The DMA receive producer controls the movement of data from the MAC to the DMA receive FIFO.

The DMA receive consumer allocates buffers from the free buffer list (BL), controls the transfer of bytes from the DMA receive FIFO into system memory via the EMI bus, and writes new buffer descriptors in the frame descriptor area (FDA). At the end of a received packet, the DMA receive consumer writes the frame descriptors in the FDA. The DMA receive consumer controls the generation of interrupts for received packets after the receive status information has been written to system memory.

1.5.4 Receive Alignment

The Ethernet Controller has the capability to skip a fixed number of bytes when placing received packets into buffers. The default is to skip 0 bytes, i.e. eight byte alignment. The DMA Control register can be programmed to skip 1 to 7 bytes in the first buffer used for each received packet. This is useful in aligning packets to match internal requirements, such as IP processing, decrypting, etc.

1.5.5 EMI Initialization

At system initialization time, the CSB and ADDRHI signals can be asserted to write the EMI configuration registers. This is normally done by having the system map the controller into a start-up memory address space, and having data transfers to those addresses generate the CSB and ADDRHI signals.

The registers that must be initialized include:

- ☐ EMI Command - to customize EMI capabilities.

The registers that might be initialized include:

- ☐ EMI Interrupt - to customize latency or route interrupts.

1.5.6 DMA and MAC Initialization

After EMI initialization, the internal DMA and MAC control registers are normally mapped into I/O space, or memory space, and can be read or written from the mapped space.

The registers that must be initialized include:

- ☐ DMA Transmit Frame Pointer - to initiate transmission.
- ☐ DMA Buffer List Frame Pointer - to provide buffers for reception.
- ☐ DMA Free Descriptor Area Base and Limit - to initialize receive notification area.
- ☐ DMA Transmit Polling Count - to customize polling for packets to transmit.
- ☐ DMA Transmit Threshold - to customize handling of transmit latency.
- ☐ MAC Transmit Control - to change default transmission settings.
- ☐ MAC Receive Control - to change default reception settings.
- ☐ MAC ARC Control - to customize station and multicast-group address recognition.
- ☐ MAC ARC Address and Data - to provide station address and other address filtering.
- ☐ MAC ARC Enable - to enable individual ARC entries after setup.

The registers that might be initialized include:

- ☐ MAC Control Register - to customize MAC configuration.
- ☐ DMA Transmit Burst Size - to customize transfer sizes.

1.5.7 Queue Initialization

Before starting the controller, the system needs to set up the transmit queue, the buffer list queue, and the receive descriptor area.

1.5.8 Transmit Queue Initialization

There are two modes of operation for the transmitter: batch processing and continuous polling. For batch processing, the system software sets up a linked list of frame descriptors to transmit, with the last frame descriptor containing an End-of-List (EOL) indicator. When the last frame descriptor is transmitted, the transmit frame pointer register loads the EOL indicator, and transmission terminates. Later, the system must restart transmission by storing a new value in this register.

For continuous polling, the system software sets up a linked list of frame descriptors to transmit, which ends with a dummy frame descriptor. The linked list may be initially empty, except for the dummy frame descriptor. The dummy frame descriptor is owned by the system, to prevent the controller from accessing it. When a new packet is to be transmitted, the dummy frame descriptor is overwritten.

1.5.8.1 Buffer List Initialization

The buffer list queue is initialized by setting up a linked list of frame descriptors with one or more frame descriptors, each containing a list of free buffer descriptors. The list can be any one of the following:

- ❑ A single frame descriptor, with a large number of free buffer descriptors.
- ❑ A linked list of frame descriptors.
- ❑ A circular queue, with the last frame descriptor pointing to the first frame descriptor.

For the first 2 methods the FDNext field would have the EOL bit set; for the last method the FDNext field of the last frame descriptor would point to the first frame descriptor.

1.5.8.2 Receive Descriptor Area Initialization

The receive descriptor area is initialized by writing the descriptor area base and limit registers. The controller will use these registers to initiate writing of the receive queue in the receive descriptor area.

1.5.8.3 DMA Transmission of a Frame

For each batch of frames to transmit, the system initializes the transmit queue, and writes the head of the queue into the transmit frame pointer register.

For continuous polling transmission, the list of frame descriptors is terminated by a dummy frame descriptor, which is owned by the system. When the controller reaches the dummy record, it will enter a polling mode. In this mode, the controller periodically reads the frame descriptor control (FDCTL) field, waiting for the FDOwner bit to be cleared by the system. The frequency of polling is controlled by the transmit polling counter register.

To transmit a frame in continuous polling mode, the system writes a new frame descriptor for the frame to transmit at the tail of the transmit queue. This is done by overwriting the old dummy frame descriptor,

creating a new dummy frame descriptor, and setting the next field of the old frame descriptor to the new dummy frame descriptor. The last step of the overwrite is to clear the FDOwner bit of the old frame descriptor, giving ownership to the controller.

1.5.8.4 Transmit Complete Notification

The system can obtain transmission completion information in a variety of ways:

- ☐ Request an interrupt.
- ☐ Poll the FDctl field of transmitted frame descriptors, for system ownership.
- ☐ Poll the transmit frame pointer register.

Interrupts can be requested at the end of each frame transmitted, or at the end of selected frames. When polling the transmit frame pointer register, the system call look for an invalid value (batch processing mode), or look for the address of the dummy frame descriptor (continuous polling mode).

1.5.8.5 Receiving a Frame

To enable the MAC to receive frames, system software must do the following:

- ☐ Initialize the Free Buffer List and Free Descriptor Areas.
- ☐ Write a dummy frame descriptor into the free descriptor area, setting the FDOwner bit of the FDctl field so the controller owns it.
- ☐ Initialize the receive frame pointer register to the address of the dummy frame descriptor in the free descriptor area.

There are two ways that system software can be notified about received frames:

- ☐ Request an interrupt for each frame received.
- ☐ Poll the dummy frame descriptor, looking for the FDOwner bit to be set.
- ☐ Interrupts are enabled by setting the completion interrupt enable bit of the receive control register.

Once a frame is received, the system must do the following:

- ☐ Process the frame descriptor and free it for reuse at a future time.
- ☐ Free buffers as they are returned, and add them to the Free Buffer List.

1.5.8.6 Processing Received Frame Descriptors

The Free Descriptor Area is intended to be used in a FIFO manner. However, different applications will take different amounts of time to process frames and return associated buffers. So frame descriptors allocated by the controller are copied to another area and freed in the order in which they are received, before being passed up the protocol stack.

1.5.8.7 Freeing Buffers

There are two ways that buffers may be allocated:

- ❑ Starting a new frame in a new buffer.
- ❑ Placing several frames or parts of frames in a single buffer.

The allocation mode is controlled by either the buffer fragment size register, or the frame descriptor control field. The single frame mode has the advantage of simpler memory management, but the disadvantage of less efficient memory utilization. The packed buffer mode has the advantage of more efficient memory utilization, but the disadvantage of more complex memory management.

Packed buffers require some additional managing, because of the possibility of multiple frames or fragments of frames in the same buffer area. The controller counts the number of buffers created in the same buffer area, and provides this count as the RxBDSeqN field of the BDCtl field in the Buffer Descriptor. System software can then count returned fragments, until all fragments are returned.

A buffer ID value, RxBDID, is copied from the buffer descriptors in the free buffer queue, to the buffer descriptors in the received frame queue. Up to 256 ID values are available. If more are needed, several techniques are available. One is to calculate high order bits from the buffer pointer values, which point into the buffer.

1.5.8.8 Processing Interrupts

When an interrupt occurs, it is generally on a shared interrupt line. To see if this EMI device is the source of an interrupt, system software reads the Interrupt Source register. Based on the contents of this register, the system software may need to read additional registers, such as the Transmit or Receive Status registers.

1.5.8.9 Interrupt Delay Register

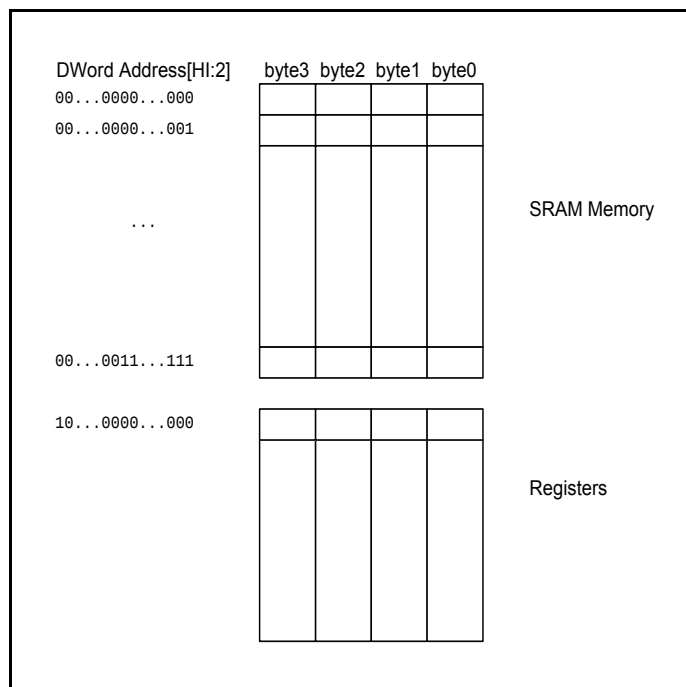
The 78Q8430 has support for delaying the occurrence of an interrupt, following the generation of an earlier interrupt.

1.6 Memory Organization and Data Structures

1.6.1 Memory Map

The EMI-based Ethernet controller provides a single address space which contains both general purpose SRAM memory, and a set of specialized control and status registers. Figure 6 shows the memory map, with low memory containing SRAM, and the upper memory containing the control and status registers.

Figure 6 : Memory Map



1.6.2 Data Structures Overview

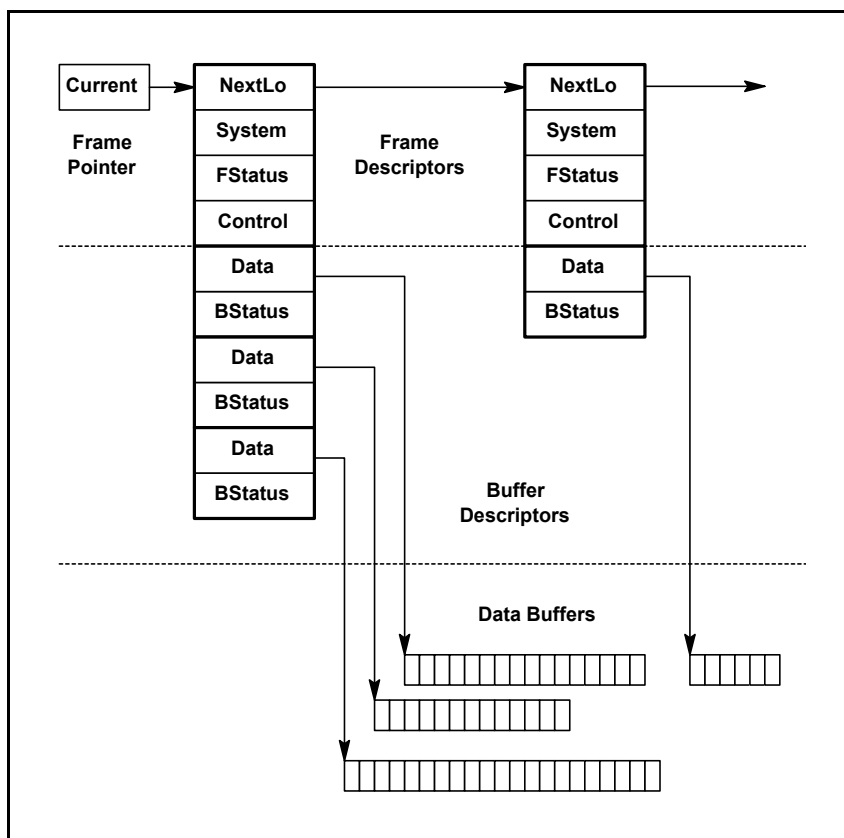
The 78Q8430 Ethernet Controller exchanges control information and data via three data structures:

- ❑ Frame descriptors.
- ❑ Buffer descriptors.
- ❑ Data buffers.

Figure 7 shows how these data structures are related. Frame descriptors have a four-byte pointer to the next frame, a four-byte system field, a frame status field, a control field for the entire frame, and an array of associated buffer descriptors. Buffer descriptors have a four-byte pointer to a data buffer and control field for the buffer. A data buffer is an array of bytes, which can be stored in either little endian or big endian order.

The DMA engine supports transfer of data on byte boundaries. Frame descriptors and buffer descriptors must be aligned on 16-byte boundaries. The DMA engine employs bursts of full four-byte, aligned transfers whenever possible. Alignment in data buffers does not affect performance very much. The DMA engine avoids doing unaligned or partial word accesses, except at the beginning or end of block transfers.

Figure 7: Data Structure Overview



1.6.3 Detailed Data Structure Formats

This section describes the data structures used by the 78Q8430 to communicate with the host system. These structures are located in system memory.

Frame descriptors, buffer descriptors, and data buffers are used in three ways:

- ❑ Transmit Queue - a list of frame descriptors for packets to transmit.
- ❑ Receive Queue - a list of frame descriptors for packets that have been received.
- ❑ Buffer List - a list of frame descriptors with unused buffers for receiving data.

Each sub-section describes one of the basic data structures. Some data structures contain different information when they are used in different queues.

In continuous polling operation, a queue does not become empty once it is active. There is always a “dummy” frame descriptor at the end of the list, which belongs to the producer of new descriptors.

To begin transmission, the system stores into the transmit frame pointer register the address of the first frame descriptor in the transmit queue. The controller traverses the transmit queue, updating the status of transmitted packets. Transmission complete is indicated in the frame descriptor status field and in the ownership bit of the frame descriptor control field. This allows the queue to be processed by system software after transmission, e.g. to free buffers.

The controller acquires buffers from the buffer list, and writes new frame descriptors and new buffer descriptors into the free descriptor area.

1.6.4 Frame Descriptor Format

Each frame descriptor has a pointer to the next frame descriptor in the queue, a system field, a status field, a control field, and a length fields. Table 4 shows the layout of a frame descriptor, as four 32-bit values.

Table 4 : Frame Descriptor Format

Byte 3	Byte 2	Byte 1	Byte 0	Offset
FDNext				00
FDSysstem				04
FDStat				08
FDctl		FDLength		0C

Table 5 : Frame Descriptor Word Definitions

FDNext	Next Frame Descriptor	Address of next frame descriptor (32 bits).
FDSysstem	Frame Descriptor System	Reserved for System use (32 bits).
FDStat	Frame Descriptor Status	Status field for this Frame Descriptor.
FDctl	Frame Descriptor Control	Control field for this Frame Descriptor.
FDLength	Frame Length	Length field for this Frame.

Each queue makes slightly different use of the FDNext, FDSysstem, FDStat, FDctl, and FDLength fields, as explained below.

1.6.4.1 Next Frame Descriptor Field (FDNext)

The next frame descriptor field contains either an End-Of-List (EOL) flag, or a pointer to the next frame descriptor in the same queue. Frame descriptors must be aligned to 16-byte boundaries, i.e. a valid pointer must have bits 0-3 set to zero.

Table 6 : Next Frame Descriptor Fields

31	4	3	2	1	0
FDNext28	0	0	0	0	EOL

FDNext28	28-bit Pointer Field	If EOL=0, contains upper 28 bits of address of the next frame descriptor in this queue.
EOL	End-Of-List Flag	=0. Pointer is valid. =1. End of list. Must wait for flag to clear.

On all the queues, the next frame descriptor field is used to stop the consumer of the list, by setting the EOL bit. The consumer must wait for the producer of the list to clear the EOL bit, when it stores a valid pointer. On the buffer list queue, it is possible to chain from one buffer pool to another using the next frame descriptor field. If chaining of buffer lists is not used, the software drivers should set the FDNext field to contain its own address. This would cause the controller to re-examine the same buffer area for re-use. Alternatively, the EOL bit can be set, causing the controller to stop.

1.6.4.2 Frame Descriptor System Field (FDSysSystem)

The FDSysSystem field is a 32-bit field which is reserved for system software use. It could be a pointer to a table of information, a pointer to C++ virtual functions, etc.

On the transmit queue, the FDSysSystem field is not used.

On the receive queue, the controller will copy the contents of the FDSysSystem field from the current buffer list queue, where the first buffer descriptor was allocated.

1.6.4.3 Frame Descriptor Status Field (FDStat)

On the transmit and receive queues, the FDStat field is used for reporting transmission and reception completion status.

On the receive free buffer list, the FDStat field is not used.

1.6.4.4 Frame Descriptor Length Field (FDLength)

On the transmit queue, the FDLength field is not used.

On the receive queue, the controller sets the FDLength field to the total length of the packet.

On the buffer list queue, the FLength field is used to count the number of free buffer descriptors allocated to the queue. The controller accesses the buffer list frame descriptor via the buffer list frame pointer register. If the controller encounters a buffer it does not own, it will set the BL_Ex bit in the Interrupt Source register and wait for the system to clear it. The controller will read the buffer descriptors, using the FLength field as a limit. When the controller nears the end of the list, it will fetch the next frame descriptor pointed to by the FDNxt field.

1.6.4.5 Frame Descriptor Control Field (FDctl)

The table below shows the abbreviation, field name, description, and usage of the FDctl field:

Table 7 : Frame Descriptor Control DWord

15	14	13	12	11	10	9		5	4		0
COWnsFD		FrmOpt				Reserved				BDCCount	

Symbol	Name	Description	Used by
COWnsFD	Controller Owns Frame Descriptor	=1. The controller owns the frame descriptor, after the system sets COWnsFD. =0. The system owns the frame descriptor, after the controller clears COWnsFD.	Tx, Rx
FrmOpt	Frame Options	Per Frame Control Options. See below.	Tx
BDCCount	Buffer Descriptor Count	Number of BD's. (1 to 29)	Tx, Rx

The ownership field is used in the transmit and receive queues to synchronize processing by the controller and the system. Frame options are used in the transmit queue and the buffer list. The buffer descriptor count field is only used in the transmit and receive queues. (The buffer list uses the length field as a count field to allow larger buffer pools). If an attempt is made to use more than 28 buffer descriptors for a single received packet, then an Excess Buffer Descriptor error is generated.

The transmit queue uses the frame options field to set transmit characteristics for individual packets:

- ☐ 10000 = Big Endian byte ordering.
- ☐ 01000 = Interrupt after transmitting.
- ☐ 00100 = No CRC appended.
- ☐ 00010 = No PAD bytes, if short frame.

These bits can be combined to ask for combinations of characteristics. For example, 01110 would mean: little endian, interrupt after transmission, do not append CRC, and do not pad a short packet.

Per packet Big Endian controls can be useful in a hub application, where packets are received for transmission from a mixture of big and little endian sources. For computer applications, it is easier to use the global big endian control bit.

1.6.5 Buffer Descriptors

Each buffer descriptor has a pointer to the data buffer, control and status bytes, and a two-byte length field. Table 8 shows the layout of a buffer descriptor.

Table 8 : Buffer Descriptor Format

Byte 3	Byte 2	Byte 1	Byte 0	Offset
BuffData				00
BDCtl	BDStat	BuffLength		04

BuffData	Buffer Data Pointer	32-bit address of storage for bytes of data.
BDCtl	Buffer Descriptor Control	Control for this buffer descriptor.
BDStat	Buffer Descriptor Status	Status for this buffer descriptor.
BuffLength	Buffer Length	Length field for this buffer descriptor.

When buffers are on the buffer list queue, the BuffData field points to the beginning of the buffer, and the BuffLength field reflects the allocated size of the unused buffer. When buffers are in use on the transmit and receive queues, the BuffData field points to the beginning of data, and the BuffLength field reflects the length of the data. The Reserved field should be written as 0, and ignored on read by the device driver.

It is the responsibility of the system software to set the length field to the allocated size, when buffers are placed in the buffer list queue. As with frame descriptors, each queue makes slightly different use of the BDCtl and BDStat fields, as explained below.

1.6.5.1 Buffer Descriptor Control (BDCtl)

On the transmit queue, the BDCtl field is not used. On the receive frame descriptor area (FDA) and buffer free list (BL) the BDCtl field indicates the current owner of the buffer: controller or device S/W driver.

Table 9 : Buffer Descriptor Control Dword

7	6	0
COWnsBD	Reserved (0)	

COWnsBD	Controller Owns Buffer Descriptor	=1. Controller owns the buffer descriptor. When the device driver sets COWnsBD, the buffer is free for reception. =0. Device driver owns the buffer descriptor. When the controller clears COWnsBD, the buffer has been filled.
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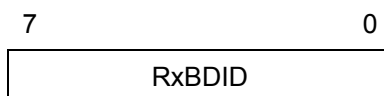
This allows synchronizing allocation and freeing of buffer descriptors, to ensure that the controller will not “wrap around” and begin reusing buffers before the system can empty them.

1.6.5.2 Buffer Descriptor Status Field (BDStat)

On the transmit queue, the BDStat field is not used by the controller.

On the receive queue, the BDStat field is used as a Buffer ID, which is copied from the free buffer queue.

Table 10 : Buffer Descriptor Status Dword



RxBDID Receive Buffer Descriptor ID The buffer ID value.

On the free buffer queue the BDStat field is used to pass the buffer descriptor ID number to the controller.

Note: Buffer IDs can only be unique if there are at most 256 buffers in a single buffer pool.

1.7 MAC Functions

Figure 4 shows an overview of the major functional blocks of the 10/100 Media Access Controller (MAC) used in the 78Q8430 controller. The MAC consists of a transmit block, a receive block, control and status registers, a flow control block, an RMON block and a serial controller for the optional external EEPROM/ROM. The MAC also has a loop back circuit.

1.7.1 MAC Transmit Block

The MAC transmit block moves the outgoing data from the MAC transmit FIFO, encapsulates it, and passes it on to the MII interface logic in the PHY. The transmit block has circuits for generating preamble and jam bytes, pad bytes, the CRC value, and error extension. The transmit block also has logic to check parity, a timer for the backoff delay after a collision, and a timer for the inter-packet gap after a transmission.

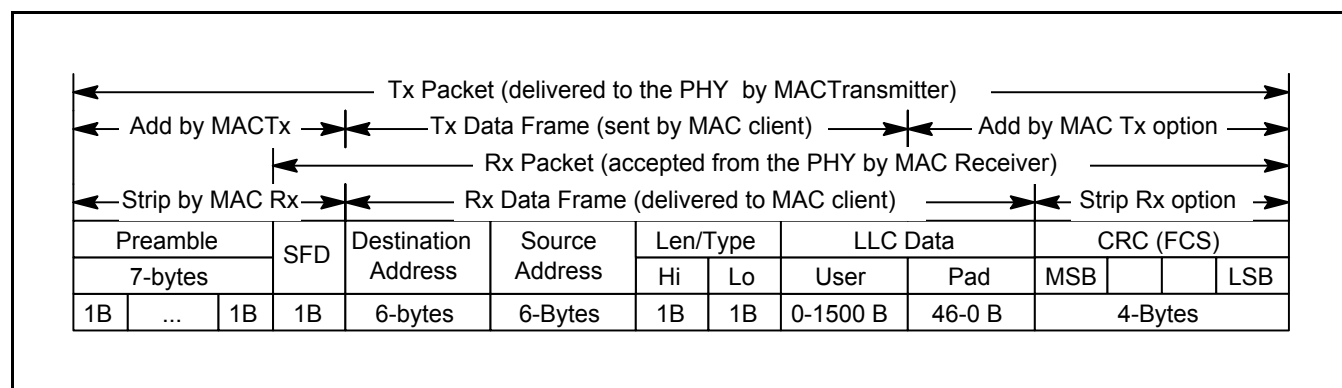
1.7.2 MAC Receive Block

The receive block de-capsules the received packet from the PHY and stores it in the MAC receive FIFO. The receive block has circuits for checking the CRC value, generating parity to protect data in the FIFO, and checking packet lengths. The receive block also has an Address Recognition Circuit (ARC) block which provides for acceptance or rejection of a packet based on its destination address.

1.7.3 MAC Frame / Packet Formats

Figure 8 shows the format of an IEEE 802.3 Ethernet packet or frame.

Figure 8 : MAC Frame / Packet Diagram



- ❑ Preamble—seven identical bytes. The bits in each byte are 10101010, transmitted from left to right. The preamble may be shortened during transmission, and is not required for reception.
- ❑ Start Frame Delimiter (SFD)—one byte. The bits are 10101011, transmitted from left to right. Required for reception.
- ❑ Destination Address—six bytes. May be an individual or a multicast address. The ARC provides optional address filtering using the Destination Address.
- ❑ Source Address—six bytes. MAC does not interpret the source address.
- ❑ Length or Type Field—two bytes. The high-order byte is transmitted first. The IEEE 802.3 Standard specifies that values less than or equal to 1500 are lengths and values greater than 1535 are types. Length values indicate the number of Logical Link Control (LLC) data bytes in the data field. The Stand-alone MAC recognizes several special values: 8808h is for MAC Control Frames and 8100h for tagged VLAN frames.
- ❑ Logical Link Control (LLC) Data—46 to 1500 bytes. The LLC data is made up of two fields: User Data and Pad Data.
- ❑ User Data - 0 to 1500 bytes.
- ❑ Pad—0 to 46 bytes. If the User Data is less than 46 bytes long, the MAC has an option to generate pad bytes to make the LLC Data field be 46 bytes long.
- ❑ Cyclic Redundancy Check (CRC)—four bytes. Also called the Frame Check Sequence, or FCS. A value computed as a function of all fields except the preamble, the SFD, and the CRC itself.

The Preamble, SFD, Pad Data, and CRC are added by the transmitter. Padding can also be done in software. There is a Transmit Control bit to suppress CRC addition. The Receive Control register has bits to control checking and stripping the CRC. Stripping of Pad Data is the responsibility of the DMA engine or software drivers.

The MAC transmits the least significant bit of each byte first for all fields except the CRC. Throughout this document, we use “packet” to denote all of the bytes transmitted and received, while “frame” refers to the bytes delivered by the user for transmission, and to the user who is receiving.

There are a number of factors and options which can affect this standard IEEE 802.3 frame:

- ❑ Some PHYs may deliver a longer or shorter preamble. Preamble may shrink due to repeaters. The transmitter sends the standard format. The receiver accepts zero or more preamble bytes, followed by SFD.
- ❑ Short packet mode allows LLC data fields with less than 46 bytes. There are options to suppress padding on transmit and allow reception of short packets.
- ❑ Long packet mode allows LLC data fields with more than 1500 bytes. There is an option to allow reception of long packets.
- ❑ No CRC mode suppresses the appending of a CRC field.
- ❑ Ignore CRC mode allows the reception of packets without valid CRC fields.

1.7.4 Destination Address Format

Bit 0 of the destination address is an address type designation bit. It identifies the address as either an individual or a group address. Group addresses are also called multicast addresses. Individual addresses are also called unicast addresses. The broadcast address is a special group address, namely ff-ff-ff-ff-ff in hex.

Bit 1 distinguishes between locally or globally administered addresses. For globally administered (or U, universal) addresses, the bit is set to 0. If an address is to be assigned locally, this bit is set to 1. For the broadcast address, this bit is also a 1.

Figure 9 : Destination Address First Byte Diagram

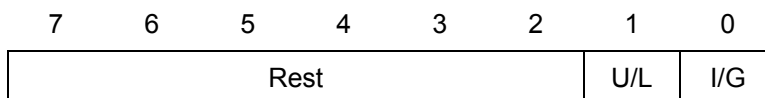


Table 11 : Destination Address (First Byte)

I/G	Individual or Group Flag	=0 Individual address. =1 Group address.
U/L	Universal or Local Flag	=0 Universal address. =1 Local address.
Rest	Rest of Byte	Rest of first byte of destination address.

1.7.5 Destination Address for Flow Control

The IEEE 802.3 Standard specifies a special destination address for use in the PAUSE Operation packets which implement full duplex Flow Control: 01-80-C2-01-00-01. In order for the MAC to receive packets which contain this special destination address, the address must be programmed into one of the ARC memory entries, that ARC memory entry must be enabled, and the ARC must be activated. Some ARC memory entries are also used when generating a Flow Control packet via the SdPause bit in the Transmit Control register, as explained later in this Chapter.

1.7.6 MAC Initialization

On power up and reset, the MAC control and status registers are set as described in Chapter 2, "Register Descriptions". Transmit Collision Count, ARC Data, and EEPROM/ROM Buffer registers are not set on power up or reset. The Transmit Collision Count register is reset at the beginning of transmitting a new packet. The ARC memory should be initialized before enabling usage of the ARC.

1.7.7 MAC Register Access

MAC Register access is controlled through the EMI bus interface. For more information on register read and write access, including MAC command and status registers, refer to Chapter 2, "Register Descriptions".

1.7.8 MAC Special Register Clear Operations

The missed packet error count register is cleared on read. This ensures synchronization with software drivers which accumulate a count total. The transmit and receive status registers are cleared at the beginning of the next packet. For this reason, the values read from the register interface may not be stable. The value of these registers is stored in the FDStatus field of the Frame Descriptor in memory for each packet transmitted or received. Software must then examine the status values found in these system data structures.

1.7.9 MAC Loopback Function

The MAC loop back circuit provides for MAC-layer testing in isolation from the PHY. This loop back function is typically used by S/W drivers to check H/W operation before enabling network access. All loopback paths originate from the EMI interface (no line side loopback).

1.7.10 Network Operation Controls

The MAC registers provide controls for network operation, including:

- ❑ Enable and disable transmit and receive circuits, including requests to halt at end of current packet.
- ❑ Interrupt enable and disable controls for individual conditions.
- ❑ Counters and status bits for collecting network management data.
- ❑ Loopback and other controls to aid in diagnosing network problems.
- ❑ Controls for reading, writing, and erasing values in an EEPROM or ROM chip.

1.7.11 Transmitting a Frame

To transmit a frame, the transmit enable bit in the transmit control register must be set and the transmit halt request bit must be zero. In addition, the halt immediate and halt request bits in the MAC control register must be cleared. These conditions are normally set after the DMA controller initialization has occurred, such as storing a valid frame descriptor address (which is stored in the transmit frame pointer register). The MAC will then signal the DMA engine to transfer bytes to the MAC transmit FIFO. The DMA transmit controller then controls the transfer of bytes to the MAC transmit FIFO.

The MAC transmit block will start transmitting the data in the FIFO. At that time, the MAC transmit block will request more data and transmit it until the DMA transmit controller signals the end of data to be transmitted. The MAC transmit block generates pad bytes if needed, appends the calculated CRC to the end of the packet, and completes the transmission. It sets the completion bit in the transmit status register, signaling the end of a transmission, which may in turn cause an interrupt.

The MAC transmit block does not begin transmission until there are eight bytes of data in the MAC transmit FIFO. Since the first eight bytes transmitted are the preamble and the Start Frame Delimiter, this gives an initial 16 byte times for DMA latency. The DMA transmit block does not begin transferring data to the MAC transmit FIFO, until either the entire packet is in the DMA RAM buffer, or the number of bytes in

the DMA RAM buffer exceeds the DMA transmit threshold register. If a transmit under run error occurs, the problem can be corrected by setting the DMA transmit threshold register to a higher value.

The MAC transmit block checks the parity. If there is a parity error, the MAC transmit block aborts the transmission, resets the FIFO, and sets the MAC parity error bit in the transmit status register.

1.7.12 IEEE 802.3 Transmit Protocols

The MAC transmit block consists of three state machines. The main transmit state machine implements the MAC-layer protocols, and controls the other two. The gap state machine tracks and counts the inter-packet gap timing between packets. A back-off state machine implements the backoff and retry algorithm of the 802.3 CSMA/CD protocol.

1.7.13 Inter-Packet Gap Timing

In half-duplex mode, the gap state machine is responsible for counting the 96 bit times from the deassertion of the carrier sense signal, which is the inter-record gap. It breaks the 96 bit times for inter-record gap into the first 64 bits, and the last 32 bits, in order to precisely control the appropriate times for beginning transmission. If there is any traffic within the first 64-bit times, it resets the counter and resumes counting from zero. If there is any traffic within the last 32 bits, it continues counting and signals the end at 96 bit times. In full-duplex mode, the gap state machine starts counting at the end of transmission and signals the end at 96 bit times (12 byte times).

1.7.14 Collision Processing and Back-off

If the main transmit state machine detects a collision, it starts the back-off state machine counters and waits for the end of the back-off slot, before retransmitting the collision-causing packet again. Each back-off slot is a multiple (including zero) of 512 bit times. Each time there is a collision for the same packet, the back-off state machine increments an internal attempt counter. A pseudo-random number generator outputs a random number by selecting a subset of the value of the generator. The subset grows by one bit for each subsequent attempt. This implements the equation:

$$0 < r < 2^k$$

$$k = \min. (n, 10)$$

where r is the number of slot times that the MAC has to wait in case of a collision, and n is the number of attempts. For example, after the first collision, n is 1 and r is a random number between 0 and 1. The pseudo-random-number generator in this case is one-bit wide and gives a random number of either 0 or 1. After the second attempt, r is a random number between 0 and 3; the state machine looks at the two least significant bits of the generator ($n = 2$) which gives a value between 0 and 3.

In order to improve the statistical independence between two MACs using the same pseudo-random number generator, the MAC uses values from the CRC of previous successfully transmitted packets to modify the basic random number sequence.

1.7.15 Transmit Operation

If there is data to be transferred, the inter-packet gap is OK, and the MII is ready (there are no collisions, and either in full-duplex mode or there is no CRS), then the MAC transmit block transmits the preamble followed by the SFD. After the transmission of the preamble and the SFD, it transmits 64 bytes of data regardless of the packet length, unless short transmission is enabled. This means that if the packet is less than 64 bytes, it will pad the LLC data field with zeroes, unless NoPad is enabled. At the end of the packet, it appends the CRC, unless NoCRC generation is enabled. If there is any collision during the first 64 bytes (8 bytes of preamble and SFD and 56 bytes of the frame), it stops the transmission and transmits a jam pattern (32 bits of all ones). It increments the collision attempt counter, returns control to the backoff state machine, and retransmits the packet when the backoff time has elapsed and the gap time is OK.

If there is a collision after the first 64 bytes, it is reported as a late collision, and the packet is terminated with an error indication. The 78Q8430 does not retry late collisions.

If there are no collisions, the MAC transmit block transmits the rest of the packet, and at this time (after the first 64 bytes have been transmitted without collisions), it allows the DMA engine to overwrite this packet. After transmitting the first 64 bytes, it transmits the rest of the packet and appends the CRC to the end. FIFO under run or more than 16 collisions will cause the state machine to abort the packet (no retry) and prepare for the next packet in the queue.

In case of any transmission errors, the MAC transmit block sets the appropriate error bit in the transmit status register, and it may generate an interrupt, depending on the transmit control register.

1.7.16 Receiving a Frame

To receive a frame, the receive enable bit in the receive control register must be set and the receive halt request bit must be zero. In addition, the halt immediate and halt request bits in the MAC control register must be cleared. These conditions are normally set after the DMA controller initialization has occurred, such as storing a valid address into the buffer list frame pointer register, and initializing the free descriptor area base and limit registers.

The MAC receive block, when enabled, constantly monitors a data stream coming from the integrated PHY. If the MAC is in loop back mode, the data stream will be coming from the MAC transmit block via internal connections.

The MAC receive block receives zero to seven bytes of preamble, followed by the Start Frame Delimiter (SFD). The MAC receive block checks that the first data received is preamble, and looks for the SFD in the first eight bytes. If the SFD is not the first non-preamble byte, it treats the packet as a fragment and discards it. The data after the SFD is the destination address. When it has received a byte, the MAC receive block generates parity, stores the byte with its parity in the MAC receive FIFO, and signals that data is present. It receives subsequent bytes and stores them in the FIFO. The DMA receive controller reads bytes from the MAC receive FIFO, checks parity, and moves the data into the DMA receive FIFO. When the MAC receive FIFO becomes empty, or when it drives out the last byte of a packet, the MAC receive block signals these conditions. If during the frame reception, the PHY asserts both Rx_DV and Rx_ER, the MAC receive block reports a CRC error for the current packet.

After the MAC receive block receives the destination address, the ARC block attempts to recognize it. If the ARC block rejects the packet, the MAC receive block signals this condition and the DMA receive block discards the data packet.

1.7.17 MAC Error Reporting

The error and abnormal operation flags set by the MAC are arranged into transmit and receive groups, and can be found in either the transmit status value or the receive status values. These values are defined in the corresponding register definitions: the transmit status register (Tx_Stat) or the receive status register (Rx_stat). In addition, the missed packet register counts packets missed for system network management purposes. Please refer to Chapter 2, "Register Descriptions," for the formats of the flags and counters.

1.7.18 MAC Transmission Errors

Transmit operation terminates when the entire packet (preamble, SFD, data, and CRC) has been successfully transmitted to the physical medium without encountering a collision. In addition, the MAC transmit block detects and reports both internal and network errors.

Under the following conditions, transmission will be aborted and a status bit will be set. Many of the bits that are set can also generate interrupts, if the corresponding interrupt enable bit has been set in the transmit control register.

1.7.18.1 Transmit Parity Error

A parity bit protects data coming from the DMA transmit controller via the DII into the MAC transmit FIFO. A parity error sets the TxParErr bit of the transmit status register and halts the transmitter, if interrupt is enabled.

1.7.18.2 Transmit FIFO Underrun Error

The 80-byte MAC transmit FIFO is capable of handling a worst case DMA latency of 1.28ms (128 bit times, or 16 byte times), because 64 bytes are retained for possible retransmission after a collision. A MAC transmit FIFO under run usually indicates a EMI bus latency problem, since the DMA transmit controller has more than enough bandwidth to keep up.

Such an under run sets the Underrun bit in the transmit status register.

1.7.18.3 Lost Carrier Error

In half duplex mode Carrier Sense (CRS) is monitored from the beginning of the Start Frame Delimiter (SFD) to the last byte transmitted. A lost carrier condition indicates that CRS was never present or was dropped during transmission (a possible network problem), but transmission is not aborted. During loop back mode, TX_EN drives CRS. During full-duplex operation, CRS is not passed to the transmit block, and lost carrier will not be asserted. Lost carrier sets the LostCRS bit in the transmit status register.

1.7.18.4 Excessive Collision Error

In half duplex mode, whenever the MAC encounters a collision during transmit, it will back off, update the collision counter, and try again later. When the counter equals 16 (all 16 attempts resulted in a collision) transmission is aborted. Excessive collisions probably indicate a network problem. Excessive collision sets the ExColl bit in the transmit status register.

1.7.18.5 Late Collision Error (Transmit Out-Of-Window Collision)

In a correctly configured and operating network, the controller sees a collision (if there is one) within the first 64 bytes of data being transmitted. If a collision occurs after this time a possible network problem is detected. Late collision sets the LateColl bit in the transmit status register, and transmission of the packet is aborted, i.e. late collisions are not retried.

1.7.18.6 Signal Quality Error

In 10 Mb/s mode, the MAC checks for a “heartbeat” at the end of a transmitted packet. This is a short Collision signal within the first 40 bit times after end of transmission. Signal Quality Error sets the SQErr bit in the Transmit Status register.

1.7.18.7 Deferral

In half duplex mode, during any attempt to send a packet, the MAC may have to defer the transmission because of a pre-occupied network. This is not an error, but is used as a network activity indicator, but only when collisions do not occur. Deferral sets the TxDeferred bit of the transmit status register.

1.7.18.8 Excessive Deferral

During the first attempt of sending a packet, the MAC may have to defer the transmission because of network activity. If the deferral time is longer than two maximum sized packet times (2.4288ms for 10-Mbit/s operation or 0.24288ms for 100-Mbit/s operation) the ExDefer bit of the transmit status register, is set, but transmission is not aborted. The MAC waits for the excessive deferral event to be cleared. Excessive deferral indicates a possible network problem. The Excessive deferral interrupt can be signaled before the packet transmission is completed, and is reported in the IntSrc register.

1.7.18.9 Paused

During any attempt to send a packet, the MAC may have to defer the transmission because the Transmitter has been paused by the reception of a MAC Control packet containing a PAUSE Operation. This is not an error, but is used as a network activity indicator.

To assist software in marking packets which experience a pause, the Paused bit is set on the last packet before a PAUSE will take effect.

1.7.19 MAC Receive Errors

The MAC receive block starts putting received data from the physical medium into the MAC receive FIFO after detecting the Start Frame Delimiter (SFD). It also checks for MAC receive FIFO overflow during reception. At the end of reception, the MAC receive block looks for external errors (Alignment, CRC, Frame Too Long, and Frame Length).

1.7.19.1 Receive Parity Error

A parity bit protects data once it enters the MAC receive FIFO. A parity error sets the RxParErr bit of the receive status register and halts the receiver, if interrupt is enabled.

CRC, Frame Alignment, and Length errors are the network errors detected by the receive unit. They might be detected in the following combinations.

- ☐ CRC error only.
- ☐ Frame Alignment and CRC errors only.
- ☐ Length and CRC errors only.
- ☐ Frame Alignment, Length, and CRC errors.

1.7.19.2 Alignment Error

At the end of reception, the MAC receive block checks that the incoming packet has been correctly framed on an 8-bit boundary. If it is not, and the CRC is invalid, data has been disrupted through the network, and the MAC receive block reports an alignment error. A CRC error is also reported. The AlignErr bit and the CRCErr bits are set in the receive status register.

1.7.19.3 CRC Error

At the end of reception, the MAC receive block checks the CRC for validity, and reports a CRC error if it is invalid.

1.7.19.4 Overflow Error

During reception, incoming data is put into the MAC receive FIFO before it is transferred to the DMA receive controller. If the MAC receive FIFO fills up because of excessive system latency or other reasons, the MAC receive block sets the Overflow Error bit of the receive status register.

1.7.19.5 Long Error

The MAC receive block checks the length of the incoming packet at the end of reception. If the length is longer than the maximum frame size of 1518 bytes, (1522 for VLAN tagged packets), the MAC receive block reports receiving a Long Error, unless long frame mode is enabled.

1.7.19.6 MII Error

The PHY informs the MAC if it detects a media error (such as coding violation) by asserting Rx_ER. When the MAC sees Rx_ER asserted, it rejects the received packet. A CRC Error is forced, and the packet is terminated. Alignment Error or Short Error may also be detected.

1.7.20 Address Recognition Circuit

The Address Recognition Circuit (ARC) supports:

- ☐ Recognition and filtering of individual, group (multi-cast), and broadcast addresses.
- ☐ Positive or Negative filtering.
- ☐ Address recognition controls, for up to 21 individual addresses.
- ☐ Promiscuous mode for network monitoring.

To read or write the ARC memory, system software should first set the ARC address register, then read or write the ARC data register. All bytes are written, without regard to partial word enables. When writing the upper or lower two bytes of a double word, it is the responsibility of the driver software to correctly write the adjacent two byte field, as well. The controller does not support read/modify/write cycles to its internal DMA RAM.

Figure 10 shows how ARC entries are formatted in control memory in the 78Q8430. Entries are assumed to be in Big endian order: #0-0 is the first byte of the first entry, #0-5 is the sixth and last byte of the first entry, and so on. There are two bytes of memory reserved after each entry. These should be written as 0 by the device S/W driver, and ignored when read. The two reserved bytes after ARC entry #7, Rsv-2 and Rsv-3, and the two double words, MC1 and MC2, are not used in ARC operation, but are used in generating MAC Control Frames.

Figure 10 : Address Recognition Circuit Memory Map

Byte 3	Byte 2	Byte 1	Byte 0	
#0-0	#0-1	#0-2	#0-3	00
#0-4	#0-5	#1-0	#1-1	04
#1-2	#1-3	#1-4	#1-5	08
#2-0	#2-1	#2-1	#2-3	0C
#2-4	#2-5	#3-0	#3-1	10
#3-2	#3-3	#3-4	#3-5	14
#4-0	#4-1	#4-2	#4-3	18
#4-4	#4-5	#5-0	#5-1	1C
#5-2	#5-3	#5-4	#5-5	20
				...
#18-0	#18-1	#18-2	#18-3	6C
#18-4	#18-5	#19-0	#19-1	70
#19-2	#19-3	#19-4	#19-5	74
#20-0	#20-1	#20-2	#20-3	78
#20-4	#20-5	Rsv-2	Rsv-3	7C
MC1-0	MC1-1	MC1-2	MC1-3	80
MC2-0	MC2-1	MC2-2	MC2-3	84

1.7.21 Full Duplex Pause Operation

The Flow Control block supports:

- ☐ Recognition of MAC Control frames received by the receive block.
- ☐ Controls to enable transmit pause on receipt of MAC Control packets specifying a PAUSE operation.
- ☐ Transmission of MAC Control frames, even if transmitter is paused.
- ☐ MAC Control packet transmit controls, to enable sending PAUSE and other MAC Control packets.
- ☐ Pass through controls, for passing MAC Control frames through to S/W drivers.
- ☐ Timers and counters for PAUSE operation.
- ☐ Command and Status Register interface.

The receive logic in the flow control block recognizes a MAC Control frame and performs the PAUSE Operation as follows: First, the length/type field must have the special value specified for MAC Control frames. Second, the destination address must be recognized by the ARC. Third, the frame length must be 64 bytes, including CRC. Fourth, the CRC must be good. And fifth, the frame must contain a valid PAUSE operation code and operand value.

If the length/type field does not have the special value specified for MAC Control frames, then the MAC takes no action, and the packet is treated as a normal packet. If the ARC does not recognize the destination address, the MAC rejects the packet. If the packet length is not 64 bytes, including CRC, the MAC will not perform the operation. The packet will be marked as a MAC Control packet, and passed forward to the S/W drivers, if pass through is enabled.

A control bit in the Transmit Status register can be set to generate a Full Duplex PAUSE Operation or other MAC Control function, even if the transmitter itself is paused.

There are two timers and corresponding CSR registers which are used during PAUSE operation. One timer and register are used when a received packet causes the transmitter to be paused. The other pair is used to approximate the pause status of the other end of the link, after the transmitter sends a PAUSE command.

The Command and Status Register (CSR) interface provides control and status bits within the transmit and receive control registers and status registers. These allow the initiation of sending a MAC Control frame, enabling and disabling MAC Control functions, and reading of the Flow Control counters.

Control bits are provided for either processing MAC Control frames entirely within the controller, or for passing MAC Control frames on to the S/W drivers. This allows Flow Control to be enabled by default even on S/W drivers which are not otherwise "Flow Control aware".

1.7.22 Local Pause Operation

To enable Full Duplex PAUSE Operation, the Special Multicast address for MAC Control Packets must be programmed into the ARC memory, and the corresponding ARC Enable bit set. While this can be any ARC location, the next section will specify how some ARC locations may be preferred, to optimize ARC entry utilization. The MAC Receive circuit recognizes the Full Duplex PAUSE Operation when the following conditions are met:

- ❑ The Type/Length field has the Special value for MAC Control packets, 0x8808.
- ❑ The packet is recognized by the ARC.
- ❑ The length of the packet is 64 bytes.
- ❑ The operation field specifies PAUSE operation, 0x0001.

When a Full Duplex PAUSE Operation is recognized, the MAC Receive circuit loads the operand value into the Pause Count Register, and signals both the MAC and the DMA engine that pause should begin at the end of the current packet, if any.

The Pause circuit maintains the Pause Counter, and decrements it to zero, before signalling the end of the pause operation, and allowing the Transmit circuit to resume.

If a second Full Duplex PAUSE Operation is recognized while the first operation is in effect, the Pause Counter is reset with the current operand value. Note that a value of 0 may cause pre-mature termination of a pause operation in progress.

1.7.23 Remote Pause Operation

The 78Q8430 Ethernet Controller supports full programmability of MAC Control frames to support both PAUSE Operation and future uses of MAC Control.

To send a remote PAUSE Operation or other MAC Control Frame the following steps need to be taken:

- ❑ Program ARC location #0 with the Destination Address.
- ❑ Program ARC location #1 with the Source Address.
- ❑ Program ARC location #7 with: the Type/Length field with the special MAC Control Type value, 0x8808; PAUSE Operation opcode, 0x0001; and operand value (duration of pause, 0x0000 to 0xffff).
- ❑ Program the two bytes after ARC location #7, Rsv-2 and Rsv-3, with 0000h.
- ❑ Program the two double word locations MC1 and MC2 with 0000_0000h.

Once these steps have been taken, sending a remote PAUSE can be accomplished in one bus operation:

- ❑ Write the Transmit Control Register, setting the SdPause bit.

The Destination Address and Source Address are normally the Special Multicast Address for MAC Control Frames and the local Station Address, respectively. These ARC entries can be enabled for use in address filtering. ARC entry #7 should not be enabled, when used as part of Flow Control transmission, since it does not contain a valid network address.

Upon completion, the transmit status is written to the Transmit Control Frame Status register. The DMA engine generates an interrupt if the Transmit Control Complete Enable bit (10) of the Interrupt Enable control register is set.

1.7.24 Pause Operation with Auto-Negotiation

The 78Q8430 has full support for PAUSE Operation in Full Duplex mode, as Specified in IEEE 802.3-2000 Annex 31.B. The PHY auto-negotiation mechanism provides for support for local and link partner capabilities in support of PAUSE (A5 - PAUSE operation, and A6 - Asymmetric PAUSE operation). After auto-negotiation, it is the responsibility of software drivers to load the link partner advertised capabilities and resolve the PAUSE capabilities. Refer to the PHY Operations chapter for additional information on advertising PAUSE support to the remote link partner.

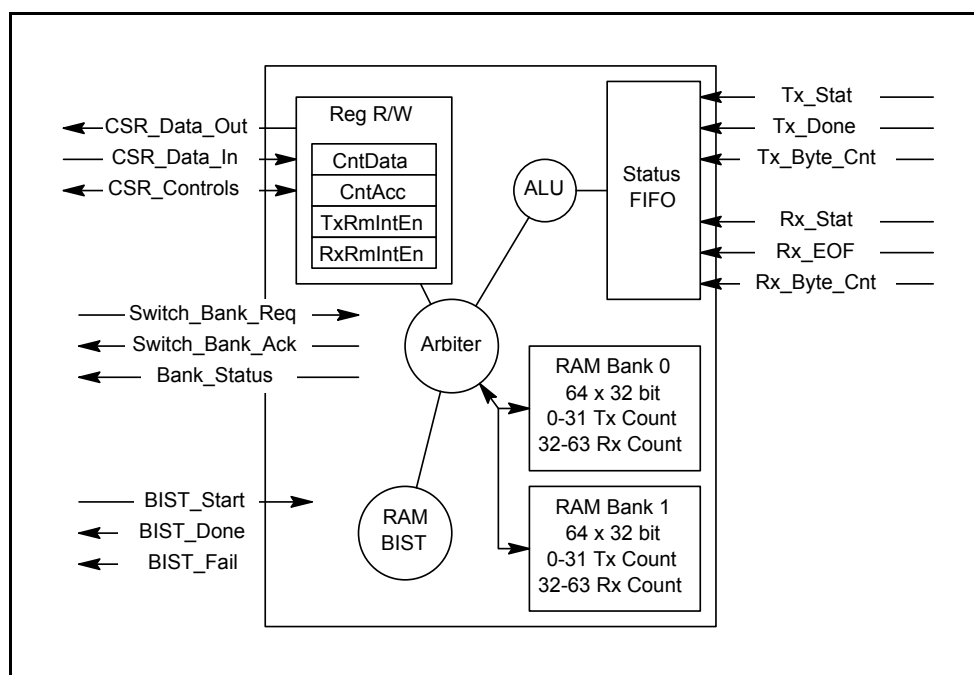
1.8 Network Statistics (RMON) Block

The Network Statistics (RMON) block provides hardware counters to accumulate statistical information for network management software. These counters support RMON, SNMP, and other popular network management software requirements.

The RMON block provides the following functions:

- ❑ Accept and buffer transmit and receive status information.
- ❑ Update counter registers with transmit and receive data flow and status events.
- ❑ Provide control and status signals for switching RAM banks 0 and 1.
- ❑ Provide read/write access via CSR to the bank not in use by the RMON logic.
- ❑ Generate interrupts based on counter roll-over events.
- ❑ Provide status information about counter roll-over events.
- ❑ Provide interrupt enable controls to use counter registers for network alerts.
- ❑ Hardware support to clear a count register to 0 when read. (Other initial values must be written by software.)
- ❑ Provide Built-in Self Test (BIST) of memory block for counters.

Figure 11 : RMON Block Diagram



On the network side, there is a FIFO for storing transmit and receive Status values. The arithmetic logic unit (ALU) supports incrementing counters and summing byte counts. Two 64 word by 32 bit RAM block provide for two banks of counter values. There is a block for doing built-in self test (BIST) and default initialization of the RAM. The Register block supports reading and writing of control registers. There are state machines to support bank switching, RAM arbitration, and overall control of the RMON block.

1.8.1 RMON Operation

The RMON module is designed to capture MAC events and relieve the system processor and software drivers of the responsibility of maintaining statistics for a managed Ethernet port. It has an internal ALU for adding and incrementing, and two memory blocks for storing the counts. Counter registers can be used as Hardware alerts. There are Interrupt Enable bits for controlling which alerts are active. Before switching counter banks, software must set up the initial values of the counters. This can be done by following a Read operation with a Write operation, to provide a non-zero starting value. Setting a counter near the roll over value provides for a quicker alert response. All counters are 32-bits, unless indicated otherwise. A counter hardware alert is generated when the counter rolls over to zero. The counter only increments. Therefore, software must initialize the counter if an alert is desired for less than 2^{32} counts.

1.8.2 RMON Transmit Counters

The RMON Block supports the transmit H/W counters defined below. Figure 12 gives a summary of the transmit counter layout, assuming a Little Endian memory map. Addresses are given in hex.

Figure 12 : RMON Transmit Counters Memory Map

Byte 3	Byte 2	Byte 1	Byte 0	
CollisionFrames[0:16]				00
FramesWithDeferredXmissions				11
LateCollisions				12
FramesLostDueToIntMACXmitError				13
CarrierSenseErrors				14
FramesWithExcessiveDeferral				15
UnicastFramesXmittedOK				16
MulticastFramesXmittedOK				17
BroadcastFramesXmittedOK				18
SQETestErrors				19
PAUSEMACCtlFramesTransmitted				1A
MACControlFramesTransmitted				1B
VLANFramesTransmitted				1C
OctetsTransmittedOK				1D
Reserved (OctetsTransmittedOKHi)				1E
Reserved				1F

Table 12 : RMON Transmit Counter Addresses

Counter Name	Addr	Description
CollisionFrames[0:16]	00h- 10h	A vector of seventeen counters, each recording the number of packets transmitted which experienced 0, 1, 2,..., 15, or 16 (excessive) collisions. For 0,..., 15, the packet was transmitted successfully. For 16 the packet was aborted due to excessive collisions. For 0 collisions, either CollisionFrames(0) or FramesWithDeferredXmissions is incremented, depending on whether deferral occurred.
FramesWithDeferredXmissions	11h	Counts each packet with no collision, which experienced delay because the medium was busy.
LateCollisions	12h	Counts each packet which experiences a late collision.
FramesLostDueToIntMACXmitError	13h	Counts each packet aborted due to underflow, parity error, or halted in middle of packet. This counter is not incremented if other error counters are incremented.
CarrierSenseErrors	14h	Counts each packet transmitted which experiences no carrier sense, or dropped carrier sense during transmission.
FramesWithExcessiveDeferral	15h	Counts each packet transmitted which experiences excessive deferral.
UnicastFramesTransmittedOK	16h	Counts each frame transmitted to unicast address.
MulticastFramesXmittedOK	17h	Counts each frame sent to a group address which is not broadcast address.
BroadcastFramesXmittedOK	18h	Counts each frame sent to a broadcast address.
SQETestErrors	19h	Counts each frame transmitted for which the SQErr flag was set. SQE Testing is only part of 10 Mb/s operation, and is not supported by 100 Mb/s PHYs.
PAUSEMACCtrlFramesTransmitted	1Ah	Counts each MAC Control Frame with PAUSE operand transmitted.
MACControlFramesTransmitted	1Bh	Counts each MAC Control Frames transmitted, which does not have PAUSE operand.
VLANFramesTransmitted	1Ch	Counts each VLAN Tagged Frame transmitted.
OctetsTransmittedOK	1Dh	Increased by the number of bytes transmitted after each successfully transmitted packet.
Reserved (OctetsTransmittedOKHi)	1Eh	Upper bits of OctetsTransmittedOK counter. Reserved for compatibility with 1G and 10G MACs.
Reserved	1Fh	

The IEEE 802.3 names have the letter “a” as a prefix. Some related counters are defined as follows:

- ❑ CollisionFrames(0) + FramesWithDeferredXmissions + FramesWithExcessiveDeferral = NoCollisionFrames.
- ❑ CollisionFrames(1) = SingleCollisionFrames.
- ❑ Sum of CollisionFrames (2 through 15) = MultipleCollisionFrames.
- ❑ CollisionFrames(16) = FramesAbortedDueToXSColls.

The current H/W does not increment Coll field on late collisions, and always terminates transmission on a late collision.

If a late collision occurs after N valid collisions, $0 < N < 16$, the CollisionFrames[N] counter is not incremented.

1.8.3 RMON Transmit Operation Summary

For each successfully transmitted packet, the RMON block updates three or four counters:

- ❑ OctetsTransmittedOK.
- ❑ One of CollisionFrames or FramesWithExcessiveDeferral or FramesWithDeferredXmissions.
- ❑ One of UnicastTransmittedOK, MulticastFramesXmittedOK or BroadcastFramesXmittedOK.
- ❑ Zero or one of PauseFramesXmitted, MACControlFramesXmitted or VLANFramesXmitted.

For each attempted transmission that ends in error, the RMON block updates one or two counters:

- ❑ One of CollisionFrames(16), LateCollisions, FramesLostDueToIntMACError, or CarrierSenseErrors.
- ❑ Zero or one of SQETestErrors (for 10 Mb/s operation only).

1.8.4 RMON Receive Counters

The RMON Block supports the following receive H/W counters. If the counter has a different IEEE 802.3 name, the name is indicated in square brackets, without the prefix "a". Receive counter addresses are given in hex. Figure 13 shows the memory map for the receive counters, assuming a Little Endian memory map:

Figure 13 : RMON Receive Counters Memory Map

Byte 3	Byte 2	Byte 1	Byte 0	
ReceivePacketSizes[0:7]				20
FrameCheckSequenceErrors				28
AlignmentErrors				29
Fragments				2A
Jabbers				2B
FramesLostDueToIntMACRcvError				2C
UnicastFramesReceivedOK				2D
MulticastFramesReceivedOK				2E
BroadcastFramesReceivedOK				2F
InRangeLengthErrors				30
OutOfRangeLengthErrors				31
VLANFramesReceived				32
PAUSEMACCtlFramesReceived				33
MACControlFramesReceived				34
OctetsReceivedOK				35
OctetsReceivedOKHi				36
OctetsReceivedOther				37
OctetsReceivedOtherHi				36
Reserved				

Table 13 : RMON Receive Counter Addresses

Name	Addr	Description
ReceivePacketSizes[0:7]	20h- 27h	An array of eight counters. Each counter counts good packets, grouped by packet size. (see below)
FrameCheckSequenceErrors	28h	Counts each frame with FCS error and without dribble.
AlignmentErrors	29h	Counts each frame with dribble and FCS error.
Fragments	2Ah	Counts each frame with less than 64 bytes, with FCS or Alignment errors.
Jabbers	2Bh	Counts each frame with more than allowed bytes (1518 or 1522 VLAN tagged), with FCS or Alignment errors.
FramesLostDueToIntMACRcvError	2Ch	Counts each frame lost due to overrun, parity error, or buffer not available.
UnicastFramesReceivedOK	2Dh	Counts each frame with a unicast address and no error.
MulticastFramesReceivedOK	2Eh	Counts each frame with no error and with a multicast address that is not the broadcast address.
BroadcastFramesReceivedOK	2Fh	Counts each frame with no error and the broadcast address.
InRangeLengthErrors	30h	Counts each frame with 1.) a length field between the minimum unpadded LLC data size and the maximum allowed LLC data size, inclusive, where the number of LLC data bytes received does not match, plus 2.) the number of frames with length field less than the minimum unpadded LLC data size and packet size not equal to 64.
OutOfRangeLengthErrors	31h	Counts each frame with length field greater than maximum allowed LLC data size, except for tags recognized by the MAC.
VLANFramesReceived	32h	Counts each VLAN tagged frame received.
PAUSEMACCtrlFramesReceived	33h	Counts each MAC Control frame with PAUSE operation code.
MACControlFramesReceived	34h	Counts each MAC Control frame without PAUSE operation code.
OctetsReceivedOK	35h	Increased by the number of packet bytes received, including padding, when there is no error and the packet is accepted.
Reserved (OctetsReceivedOKHi)	36h	Upper bits of 48-bit OctetsReceivedOK counter.
OctetsReceivedOther	37h	Increased by readable frame bytes received, and not counted under OctetsReceivedOK.
Reserved (OctetsReceivedOtherHi)	38h	Upper bits of OctetsReceivedOther counter. Reserved for compatibility with higher speed MACs.
Reserved	39h- 3Fh	

The index values for ReceivePacketSizes(0:7) are calculated as follows:

- ❑ ReceivePacketSizes(0) - Pkts63orLess - packets of 63 bytes or less.
- ❑ ReceivePacketSizes(1) - Pkts64Octets - packets with exactly 64 bytes.
- ❑ ReceivePacketSizes(2) - Pkts65to127Octets - packets of 65 to 127 bytes.
- ❑ ReceivePacketSizes(3) - Pkts128to255Octets - packets of 128 to 255 bytes.
- ❑ ReceivePacketSizes(4) - Pkts256to511Octets - packets of 256 to 511 bytes.
- ❑ ReceivePacketSizes(5) - Pkts512to1023Octets - packets of 512 to 1023 bytes.
- ❑ ReceivePacketSizes(6) - Pkts1024to1518Octets - 1024 to 1518 bytes (1522 for VLAN tag).
- ❑ ReceivePacketSizes(7) - FrameTooLongErrors - 1519 bytes or more (1523 or more for VLAN tag).

Good packets received which are longer than 1518 bytes (1522 for VLAN) will cause the ReceivePacketSizes (7) counter to increment, independent of how the LongEn bit in the Rx_Ctl register is set, providing there are no other errors. The LongEn bit only affects the setting of Good bit in Rx_Stat and the generation of interrupts. It does not affect the RMON block.

1.8.5 RMON Receive Operation Summary

For each successfully received packet, the RMON block updates three to four counters:

- ❑ OctetsReceivedOK.
- ❑ One of ReceivePacketSizes(0 to 7).
- ❑ One of UnicastFramesReceivedOK, MulticastFramesReceivedOK, or BroadcastFramesReceivedOK.
- ❑ Zero or one of VLANFramesReceived, PAUSEMACCtrlFramesReceived, MACControlFramesReceived, or OutOfRangeLengthErrors.

For each packet received that ends in error or rejection, the RMON block updates two or three counters:

- ❑ OctetsReceivedOther.
- ❑ One of FrameCheckSequenceErrors, AlignmentErrors, Fragments, Jabbers or FramesLostDueToIntMACRcvError.
- ❑ Zero or one of InRangeLengthErrors or OutOfRangeLengthErrors.

1.8.6 RFC 1643 Counters

The RMON Block supports the following counters, as referenced in RFC 1643, "Definitions of Managed Objects for the Ethernet-like Interface Types". This document is the base document for Ethernet definitions for SNMP and other Internet standards.

The RFC 1643 name for the counter is formed by adding "dot3Stats" to the front of the name below. The IEEE 802.3 name is formed by adding "a" to the front of the name below. If the two documents use different names, the IEEE 802.3 name is given in square brackets. The numbers represent internal counter memory addresses.

1.8.7 The "Ethernet-like" Statistics Group

AlignmentErrors - 32-bit H/W counter (29h).

FCSErrors [FrameCheckSequenceErrors] - 32-bit H/W counter (28h).

SingleCollisionFrames - 32-bit H/W counter, CollisionFrames[1] (01h).

MultipleCollisionFrames - S/W sum of fourteen 32-bit H/W counters, CollisionFrames[2] through CollisionFrames[15] (02h to 0Fh).

SQETestErrors - 32-bit H/W counter (19h).

DeferredTransmissions [FramesWithDeferredXmissions] - 32-bit H/W counter (11h).

LateCollisions - 32-bit H/W counter (12h).

ExcessiveCollisions [FramesAbortedDueToXSColls] - 32-bit H/W counter, CollisionFrames[16] (10h).

InternalMacTransmitErrors [FramesLostDueToIntMACXmitError] - 32-bit H/W counter (13h).

CarrierSenseErrors - 32-bit H/W counter (14h).

FrameTooLongs [FrameTooLongErrors] - 32-bit H/W counter (31h).

InternalMACReceiveErrors [FramesLostDueToIntMACRcvError] - 32-bit H/W counter (2Ch).

1.8.8 The “Ethernet-like” Collision Statistics Group

CollFrequencies[0:16] [CollisionFrames[0:16]] - 32-bit H/W counters (00h-10h).

1.8.9 RFC 2819 Counters

The RMON Block supports the following counters, as defined in RFC 2819, “Remote Network Monitoring Management Information Base”. This document defines the MIB for RMON.

The RFC 2819 name for the counter is formed by adding “etherStats” to the front of the name below. The IEEE 802.3 name is formed by adding “a” to the front of the name. If the two documents use different names, the IEEE 802.3 name is given in square brackets. The numbers represent internal counter memory addresses.

1.8.10 Ethernet Statistics Group

DropEvents [no IEEE counter] - 16-bit H/W counter, MissedCount. (in basic MAC).

Octets [OctetsReceivedOK+OctetsReceivedOther] - S/W sum of two 32-bit H/W counters of octets received (35h +37h).

Pkts [no IEEE equivalent] - S/W sum of PktsOK and PktsErr. PktsOK is S/W sum of three 32-bit counters, UnicastFramesReceivedOK, MulticastFramesReceivedOK, and BroadcastFramesReceivedOK, (2Dh, 2Eh, and 2Fh). PktsErr is S/W sum of five 32-bit counters, FrameCheckSequenceErrors, Alignment Errors, Fragments, Jabbers, and FramesLostDueToIntMACRcvError. (28h, 29h, 2Ah, 2Bh, and 2Ch).

BroadcastPkts [BroadcastFramesReceivedOK] - 32-bit H/W counter (2Fh).

MulticastPkts [MulticastFramesReceivedOK] - 32-bit H/W counter (2Eh).

CRCAAlignErrors [FrameCheckSequenceErrors + AlignmentErrors] - S/W sum of AlignmentErrors and FrameCheckSequenceErrors (29h and 28h).

UndersizePkts [no IEEE equivalent] - 32-bit H/W counter, Pkts63orLess, of good packets received with less than 64 bytes.(20h).

OversizePkts [FrameTooLongErrors] - 32-bit H/W counter, of good packets received with more than allowed bytes (1518 or 1522 VLAN tagged) (27h).

Fragments [no IEEE equivalent] - 32-bit H/W counter, of packets received of less than 64 bytes, with FCS or Alignment errors. (2Ah).

Jabbers [no IEEE equivalent] - 32-bit H/W counter, of packets received of more than allowed bytes (1518 or 1522 VLAN tagged), with FCS or Alignment errors. (2Bh).

Collisions(0:16) [no IEEE equivalent] - a vector of seventeen 32-bit H/W counters, CollisionFrames[0:16], each recording the number of packets transmitted which experienced 0, 1, 2,..., 15, or 16 (excessive) collisions. (00h to 10h).

Pkts64Octets [no IEEE equivalent] - 32-bit H/W counter, of good packets received with exactly 64 bytes, ReceivePacketSizes[1] - (01h).

Pkts65t0127Octets [no IEEE equivalent] - 32-bit H/W counter, of good packets received with 65 to 127 bytes, ReceivePacketSizes[2] - (02h).

Pkts128t0255Octets [no IEEE equivalent] - 32-bit H/W counter, of good packets received with 128 to 255 bytes, ReceivePacketSizes[3] - (03h).

Pkts256t0511Octets [no IEEE equivalent] - 32-bit H/W counter, of good packets received with 256 to 511 bytes, ReceivePacketSizes[4] - (04h).

Pkts512t01023Octets [no IEEE equivalent] - 32-bit H/W counter, of good packets received with 512 to 1023 bytes, ReceivePacketSizes[5] - (05h).

Pkts1024t01518Octets [no IEEE equivalent] - 32-bit H/W counter, of good packets received with 1024 to 1518 bytes (1522 bytes for VLAN), ReceivePacketSizes[6] - (06h).

1.8.11 RFC 1213 Counters

The RMON Block supports the following counters, as defined in RFC 1213, "Management Information Base for Network Management of TCP/IP-based internets: MIB-II". This document defines the second version of the MIB (MIB-II).

The RFC 1213 name for the counter is formed by adding "if" to the front of the name below. The IEEE 802.3u name is formed by adding "a" to the front of the name below, unless a different name is given in square brackets. The numbers represent internal counter addresses.

1.8.12 Interfaces Group

InOctets [no IEEE equivalent] - S/W sum of two 32-bit H/W counters, OctetsReceivedOK and OctetsReceivedOther. (35h and 37h).

The above definition includes the 14-byte header, but not the 8 bytes of preamble and SFD. If the preamble and SFD are intended to be included, then the sum needs to be adjusted, by adding 8*(Sum of ReceivePacketSizes[0] through [7] + Sum of five error counters: FrameCheckSequenceErrors, AlignmentErrors, Fragments, Jabbers, and FramesLostDueToIntMACRcvError).

InUcastPkts [no IEEE equivalent] - 32-bit H/W counter of the number of unicast packets received, UnicastFramesReceivedOK. (2Dh).

InNUcastPkts [no IEEE equivalent] - S/W sum of two 32-bit H/W counters, BroadcastFramesReceivedOK and MulticastFramesReceivedOK. (2Fh + 2Eh).

InDiscards [no IEEE equivalent] - S/W counter of packets delivered with no error, but discarded before delivery to higher level protocol. Kept by S/W drivers, but could include MissedCount (inside of MAC).

InErrors [no IEEE equivalent] - S/W sum of the five receive H/W error counters FrameCheckSequenceErrors, AlignmentErrors, FramesLostDueToIntMACRcvError, Fragments, and Jabbers. (28h, 29h, 2Ch, 2Ah, and 2Bh).

InUnknownProtos [no IEEE equivalent] - S/W count of packets discarded because of an unknown or unsupported protocol. Kept by S/W drivers, but could include MACControlFramesReceived, depending on upper protocols.

OutOctets [OctetsTransmittedOK] - 32-bit H/W counter of the total number of octets transmitted, OctetsTransmittedOK. (1Dh).

The above definition includes the 14-byte header, but not the 8 bytes of preamble and SFD. If the preamble and SFD are intended to be included, then the sum needs to be adjusted, by adding 8*(UnicastFramesXmittedOK, MulticastFramesXmittedOK, and BroadcastFramesXmittedOK).

OutUcastPkts [no IEEE equivalent] - 32-bit H/W counter of the number of unicast packets transmitted, UnicastFramesTransmittedOK. (16h).

OutNUcastPkts [no IEEE equivalent] - S/W sum of two 32-bit H/W counters, MulticastFramesXmittedOK and BroadcastFramesXmittedOK. (17h and 18h).

OutDiscards [no IEEE equivalent] - S/W counter of packets delivered with no error, but discarded before transmission. Kept by S/W drivers.

OutErrors [no IEEE equivalent] - S/W sum of the five transmit H/W error counters: ExcessiveCollisions, LateCollisions, FramesLostDueToIntMACXmitError, CarrierSenseErrors, and ExcessiveDeferral. (10h, 12h, 13h, 14h and 15h).

1.9 IP Processing

The DMA and MAC circuits are capable of generating and checking IP checksum values. For the transmit circuit, checksum generation can be enabled or disabled. For the receive circuit and the transmit circuit when generation is disabled, checksum checking can be enabled or disabled.

The 78Q8430 makes use of the IP Type Offset field of the IP Checksum Control register to locate and recognize IP Datagram packets. These packets are characterized by a type value of 0800h. For all IP Datagram packets, the 78Q8430 can generate and check the 16-bit IP Header Checksum value.

In addition to the IP Header Checksum, the 78Q8430 Transmit and Receive circuits can calculate, substitute, and check some of the protocol checksums, as indicated in the following sections.

1.9.1 TCP Processing

If the IP Header has a protocol value of 6, the IP datagram is carrying a TCP payload. The 78Q8430 will compute and substitute or check the 16-bit TCP Checksum over the TCP Header and payload.

1.9.2 UDP Processing

If the IP Header has a protocol value of 17, the IP datagram is carrying a UDP payload. The 78Q8430 will compute and substitute or check the 16-bit UDP Checksum over the UDP Header and payload.

1.10 Station Management Controller (SMC)

The 78Q8430 includes a state machine and a register interface for generating the Management Data (MDIO and MDC) signals of the MII station management entity. This provides logic for reading and writing control and status registers in Read/Write of registers in the PHY. The 78Q8430 PHY address is set to "00001".

The basic sequence of events in accessing the station management data are:

- ❑ System software reads the busy bit to ensure the SMC is not busy.
- ❑ On a write, the data should be written into the data register before setting the control register.
- ❑ Software writes the register address field, the read/write flag, and sets the busy bit in the control register.
- ❑ The controller completes the operation, and clears the busy bit.
- ❑ On a read, when system software detects the busy bit is cleared, it can read the data register.

1.11 EEPROM Controller

The PROM controller provides logic for reading and writing an optional external EEPROM or ROM device. The external devices supported are the MicroChip 93LC46B and the National NM93C46. Timing compatible devices, smaller devices, and Read-only equivalent devices are also supported.

The basic sequence of events in accessing an external EEPROM or serial ROM are:

- ❑ System software reads the busy bit to ensure the EEPROM driver is not busy.
- ❑ On a write, the data should be written into the data register before setting the control register.
- ❑ Software writes the address and the read/write flag, and sets the busy bit.
- ❑ The controller completes the operation, and clears the busy bit.
- ❑ On a read, when system software detects the busy bit is cleared, it can read the data register.

1.12 Power Modes

1.12.1 EMI Normal Mode

In mission mode the 78Q8430 Ethernet MAC can be programmed to either : 1) Interrupt on each packet or group of packets transmitted or received, and poll continuously for new packets to transmit. 2.) Post data and descriptors, but do not interrupt for packets received. An interrupt for each packet or group of packets is the traditional way that Ethernet software is controlled. This is appropriate for occasional network traffic, such as electronic mail. However, as processors increase in speed and complexity, the time to service an interrupt does not improve correspondingly. In fact, many modern processors have large amounts of state information and sophisticated caching schemes, which can slow the relative speed of interrupt processing even further. Combined with a faster network, where packets may arrive more frequently, the overhead for servicing network interrupts can become a significant burden to the system. Also, some applications, such as interactive conferences, require a much higher level of network traffic. These factors lead to the design of more efficient network control schemes.

By enabling or disabling interrupts for selected frame descriptors, and by delaying the occurrence of successive interrupts, the device S/W can arrange for the controller to process multiple packets between interrupts. This reduces the overhead in servicing interrupts, and improves performance by caching code when the system processes several packets at once. It is even possible to set up the controller so that it generates no interrupts at all unless serious errors occur. This requires enabling some additional controls, to ensure that the starting and stopping of traffic, and polling during idle times, is handled efficiently.

1.12.2 EMI Reduced Power Mode

In reduced power mode of operation, the 78Q8430 Ethernet Controller can have specific Wake Up technology enabled. The MAC and DMA engine continue to receive packets, but these packets are only processed to see if they contain wake up signals.

1.12.3 PHY Normal Operation Mode

In normal operation, the internal 78Q8430 PHY is connected to the MAC and controls MAC operation. The MAC and PHY may operate in Full Duplex or Half Duplex mode, at 100-Mbits/sec or at 10-Mbits/sec.

1.12.4 PHY Power Down Mode

The internal PHY can be powered down via the PWRDN bit in the PHY management register MR0. When the internal PHY is in power-down mode, it can still execute management transactions.

1.12.5 PHY Power Management Mode

Receive power management mode is activated by setting the RXCC bit in the PHY management register MR16. In this mode of operation, the adaptive equalizer, the clock recovery phase lock loop (PLL), and all other receive circuitry will be powered down when no valid MLT-3 signal is present at the UTP receive line interface. As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. During this mode of operation MAC receive clock will be inactive when there is no data being received. Note that the RXCC mode is not supported during 10BASE-T operation.

1.12.6 PHY Transmit High Impedance Mode

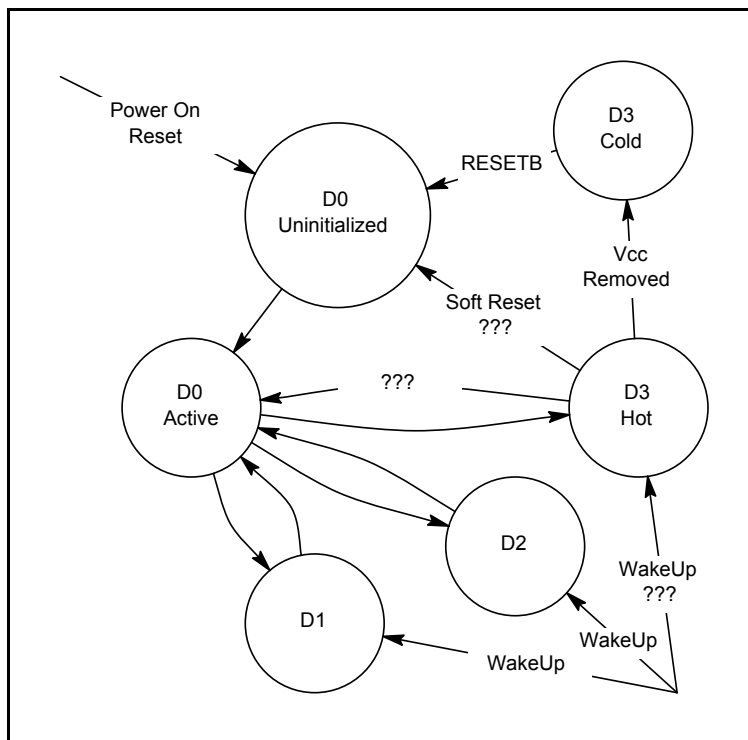
Transmit high impedance mode is activated by setting the TXHIM bit in the PHY management register MR16. In this mode of operation, the transmit UTP drivers are in a high impedance state and the internal transmit clock is held high. The receive circuitry remains fully operational. Once the TXHIM bit is cleared, the transmitter resumes normal transmit operation. The default state of the TXHIM bit is clear (transmitter active).

1.12.7 Wake Up Services

1.12.8 ACPI and EMI Power Management

The 78Q8430 supports ACPI functionality through an EMI Power Management interface. In the current design, EMI Power Management block supports network monitoring of packets for wake-up services only in the D1 state. The Controller does not support network monitoring in state D2, clock stopped, or in state D3Hot. Figure 14 shows the states and transitions supported by the current design.

Figure 14 : Current EMI Power Management States



The current implementation is fully compliant with ACPI 1.0 and 2.0. However, it does not support some features that might be desirable for mobile and advanced applications. Figure 15 shows the states and transitions of an enhanced EMI PM implementation.

The diagram illustrates a state transition logic for a system with six states: D0 Uninitialized, D0 Active, D1, D2, D3 Cold, and D3 Hot. The transitions are as follows:

- Power On Reset** leads to **D0 Uninitialized**.
- RESETB** leads to **D0 Uninitialized**.
- Soft Reset ???** leads to **D0 Uninitialized**.
- D3 Cold** transitions to **D3 Hot** when **Vcc Removed**.
- D3 Hot** transitions to **D0 Active** when **WakeUp ???** occurs.
- D3 Hot** transitions to **D2** when **WakeUp** occurs.
- D2** transitions to **D1** when **WakeUp** occurs.
- D1** transitions to **D0 Active** when **WakeUp** occurs.
- D0 Active** transitions to **D0 Uninitialized**.
- D0 Active** transitions to **D2**.
- D0 Active** transitions to **D1**.
- D0 Active** transitions to **D3 Hot** (labeled with **???**).

1.12.8.1 Magic Packet®

- ❑ Packet must be received while in a reduced power state.
- ❑ Packet must have a valid CRC.
- ❑ It must be accepted by the ARC (additional setup).
- ❑ Packet must contain the following, byte-aligned pattern.
- ❑ Six bytes containing all ones: ff-ff-ff-ff-ff in hexadecimal, followed by:
- ❑ A specified station address repeated 16 times.

The station address is specified by setting the Magic Packet Index value, to select one of the ARC entries. The ARC entry does not need to be enabled for normal use in order to be used for Magic Packet recognition, but it may be enabled.

This Magic Packet mechanism is intended to provide a remote wake-up function for sleeping machines, so they can respond to normal protocol stack operations. With appropriate auxiliary power, and alternate clock source the wake-up function can be extended to provide cold boot wake-up, as well.

1.12.8.2 OnNow Packet Pattern Matching

The controller supports OnNow pattern matching with the following features:

- ❑ Supports up to 5 OnNow patterns.
- ❑ Patterns can cover up to the first 128 bytes of a packet.
- ❑ Patterns matching for all patterns is run concurrently (checked against 5 patterns at wire speed).
- ❑ Uses the standard CRC circuit to identify pattern match.

The patterns are specified as a bit mask. The bit mask is indexed as bits 0 through 127 with each bit corresponding to the same byte index of any received packet. If the bit is a “1”, the byte is to be used in the CRC calculation. If the bit is a “0”, the byte is skipped in the CRC calculation (treated as a “don’t care” position).

Each 128-bit pattern is distributed across the OnNow Pattern Memory so that pattern checking is concurrent. As a result, all of the individual bit values corresponding to a specific byte index are found in the same pattern memory byte. The bit values are right justified, so bit 7 to bit 5 (little endian) are not used.

1.12.8.3 Memory Map for OnNow Pattern Matching

The memory map shown in Table 14 shows the mapping of packet pattern byte numbers (0 to 127 decimal) to memory locations in the ARC memory. The same registers are used to read and write both the Address Recognition Circuit (ARC) entries and the patterns for OnNow Pattern Matching.

Table 14 : OnNow Memory MAP

DECIMAL	HEX	BYTE3	BYTE 2	BYTE 1	BYTE 0
52	34	Index 003	Index 002	Index 001	Index 000
53	35	Index 007	Index 006	Index 005	Index 004
...	...	...	...	...	...
82	52	Index 123	Index 122	Index 121	Index 120
83	53	Index 127	Index 126	Index 125	Index 124

1.12.8.4 Wake-up Packet Delivery

Once a packet has caused a wake up event, through Magic Packet(tm), OnNow Pattern Matching, or External Event monitoring, the following occurs:

- ❑ Controller asserts INTB to request change to normal mode operation.
- ❑ Once restored to normal mode operation, the wake up packet can be delivered across the EMI bus.

1.12.8.5 Host Not Responding Packet

The Ethernet Controller with Wake Up support uses 32 bytes of the on-chip buffer memory to store a "Host Not Responding Packet". When INTB is asserted, a 32-bit counter is loaded from the HNR_CNT register, and decrements on each system clock cycle. If the register reaches zero before the system has caused the INTB to be deasserted, and if the Host Not Responding Control has been enabled, then the transmitter will send a Host not responding packet after completion of any current Transmit packet. The 32 bytes will be padded to a normal 64 byte packet, assuming the Transmit NoPad option is not set.

Figure 16 : Host Not Responding Memory Map

Byte 3	Byte 2	Byte 1	Byte 0	
HNR-0	HNR-1	HNR-2	HNR-3	88
HNR-4	HNR-5	HNR-6	HNR-7	8C
HNR-8	HNR-9	HNR-10	HNR-11	90
HNR-12	HNR-13	HNR-14	HNR-15	94
HNR-16	HNR-17	HNR-18	HNR-19	98
HNR-20	HNR-21	HNR-22	HNR-23	9C
HNR-24	HNR-25	HNR-26	HNR-27	A0
HNR-28	HNR-29	HNR-30	HNR-31	A4
D1C-S	D1C-D	D0C-S	D0C-D	A8
D3C-S	D3C-D	D2C-S	D2C-D	AC
D1D-S	D1D-D	D0D-S	D0D-D	B0
D3D-S	D3D-D	D2D-S	D2D-D	B4

The Bytes HNR-0 through HNR-31 are used as the first 32 bytes of the Host Not Responding Packet.

The packet is transmitted with the Padding enabled, independent of the setting of the NoPad bit.

1.12.9 Power Management and Scale Factors

The Ethernet Controller supports the reading of six Power Consumption and Power Dissipation values, and their corresponding Scale values.

The software drivers write values to a RAM override area, and enable the use of this area. An optional external EEPROM may be used to store the values for the S/W drivers. A control bit in the Wake Up Control register controls switching.

The Bytes D0C-D, D0C-S, through D3D-D, and D3D-S are:

- ☐ D0C-D means D0 power Consumed - Data,.
- ☐ D0C-S means D0 power Consumed - Scale,.
- ☐ ...
- ☐ D3D-D means D3 power Dissipated - Data.
- ☐ D3D-S means D3 power Dissipated - Scale.

The lower two bits are used for the scale factors while the upper 6 bits are ignored.

1.12.9.1 External Event Monitoring

The Ethernet Controller has the capability to monitor up to two external signals, in addition to Link Status. The controller can be enabled to wake up when one or more of these signals change status.

1.13 PHY Operations

1.13.1 Automatic MDI/MDIX Cable Crossover Configuration

The transmitter and receiver contain logic and muxing to detect and correct for cross over cabling errors. The implementation is fully compliant with IEEE 802.3 specifications, ensuring interoperability with other PHYs which may or may not implement automatic MDI/MDI-X configuration. The automatic MDI/MDI-X state machine facilitates switching TXN and TXP pins with the RXN and RXP pins, prior to the auto-negotiation mode of operation. The correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. Use of an 11-bit linear feedback shift register (LFSR) creates a pseudo-random sequence to determine the MDI configuration. Upon making the selection to either MDI or MDI-X, the 78Q8430 waits for a specified amount of time while evaluating its receive channel to determine whether the other end of the link is sending link pulses or 10BASE-T or 100BASE-TX data. If link pulses or data are detected, the 78Q8430 remains in that configuration. If link pulses or data are not detected, it increments its LFSR and makes a decision to switch based on the value of the next bit. The state machine does not move from one state to another while link pulses are being transmitted.

1.13.2 100Base-TX Transmit

The 78Q8430 PHY contains all of the necessary circuitry to convert the transmit MII signaling from a MAC to an IEEE-802.3 compliant data-stream driving Cat-5 UTP cabling. The internal PCS interface maps 4 bit nibbles from the MII to 5 bit code groups as defined in Table 24-1 of IEEE-802.3. The 5 bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse shaping circuitry and line driver. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall time in the MLT-3 signal is achieved using an accurately controlled voltage ramp generator. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer connects to the 3.3V supply.

1.13.3 100Base-TX Receive

The 78Q8430 PHY receives a 125MBaud MLT-3 signal through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The effect of these circuits is to sense the amount of dispersion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The 78Q8430 PHY can compensate for cable loss of up to 10dB at 16 MHz. This loss is represented as test_chan_5 in Annex A of the ANSI X3.263:1995 specification and corresponds to approximately 140m of CAT-5 UTP cabling. The equalized MLT-3 data signal is bidirectionally sliced and the resulting bit-stream is presented to the CDR where it is re-timed and decoded to NRZ format. The retimed serial data is converted to parallel, then descrambled and aligned into 5 bit code groups. The receive PCS interface maps these code groups to 4 bit data for the internal MII as outlined in Clause 24 of IEEE-802.3.

1.13.4 10Base-T Transmit

The 78Q8430 PHY takes 4 bit parallel NRZ data via the MII interface and passes it through a parallel to serial converter. The data is then passed through a Manchester encoder, pre-emphasis pulse-shaper, media filter, and finally to the twisted-pair line driver. The pulse shaper and filter ensures the output waveforms meet the output voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted pair media is through a center-tapped 1:1 transformer. No external filtering is required. During auto-negotiation and 10BASE-T idle periods, link pulses are transmitted.

The 78Q8430 PHY employs an on board timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer is exceeded the chip enters the jabber state, and transmission is disabled. The jabber state is exited after the MII goes idle for 500ms $\pm$ 250ms.

1.13.5 10Base-T Receive

The 78Q8430 PHY receives Manchester encoded 10BASE-T data through the twisted pair inputs and re-establishes logic levels through a slicer with a smart squelch function. The slicer automatically adjusts its level after valid data with the appropriate levels are detected. Data is passed on to the CDR where the clock is recovered, data is re-timed and passed through a Manchester decoder. From here data enters the serial to parallel converter for transmission to the MAC via the media independent interface. Interface to the twisted pair media is through a 1:1 transformer. Polarity information is detected and corrected in internal circuitry.

1.13.6 SQE Test

The 78Q8430 PHY supports the signal quality error (SQE) function detailed in IEEE-802.3. At an interval of 1 μ s after each negative transition of the TXEN pin in 10BASE-T mode, the COL pin will go high for a period of 1 μ s. SQE is not signaled if a collision is detected during transmission. This function can be disabled through register bit MR16.11.

1.13.7 Polarity Correction

The 78Q8430 PHY is capable of either automatic or manual polarity reversal for 10BASE-T and auto-negotiation. These features are controlled by the PHY management register MR16, bits APOL and RVSPOL. The default is automatic mode, where APOL is negated and RVSPOL indicates if the detection circuitry has inverted the input signal. To enter manual mode, APOL needs to be asserted, and then RVSPOL will control the signal polarity.

1.13.8 Natural Loopback

The natural loop back function can be enabled by setting register bit MR16.10. With natural loop back enabled, whenever the 78Q8430 PHY is transmitting and not receiving on the twisted pair media (10BASE-T Half Duplex mode), data on the TXD pins is looped back onto the RXD pins. During a collision, data from the RXI pins is routed to the RXD pins.

1.13.9 Auto-Negotiation

The 78Q8430 PHY supports the auto-negotiation functions of Clause 28 of IEEE-802.3. This function can be controlled via register settings. The auto-negotiation function defaults to on and bit MR0.12, ANEGEN, is high after reset. Software can disable the auto-negotiation function by writing to bit MR0.12.

The contents of register MR4 are sent to the PHY's link partner during auto-negotiation, coded in fast link pulses. Bits MR4.8:5 reflect the state of the TECH[2:0] bits after reset. If TECH[2:0] = 111, then all 4 bits are high. If TECH[2:0] = 001, then only bit 5 is high. After reset, software can change any of these bits from a 1 to a 0.

With auto-negotiation enabled, the 78Q8430 PHY will start sending fast link pulses at power on, loss of link or a command to restart. At the same time it will look for either 10BASE-T idle, 100BASE-TX idle or fast link pulses from its link partner. If either idle pattern is detected, the 78Q8430 PHY configures itself in half-duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring the acknowledge bit) the link code word is stored in register 5. Upon receiving three more identical link code words, with the acknowledge bit set, the 78Q8430 PHY configures itself to the highest priority technology common to the two link partners. The technology priorities are, in descending order:

- ❑ 100BASE-TX, Full Duplex.
- ❑ 100BASE-TX, Half Duplex.
- ❑ 10BASE-T, Full Duplex.
- ❑ 10BASE-T, Half Duplex.

Once auto-negotiation is complete, register bits MR18.11:10 will reflect the actual speed and duplex that was chosen. If auto-negotiation fails to establish a link for any reason, register bit MR18.12 will reflect this and auto negotiation will restart from the beginning. Writing a one to bit MR0.9, RANEG, will also cause auto negotiation to restart

1.13.10 Auto-Negotiation of Full Duplex Pause Operation

The 78Q8430 has full support for PAUSE Operation in Full Duplex mode, as Specified in IEEE 802.3-2000 Annex 31.B. The PHY auto-negotiation mechanism provides for support for local and link partner capabilities in support of PAUSE (A5 - PAUSE operation, and A6 - Asymmetric PAUSE operation). After auto-negotiation, it is the responsibility of software drivers to load the link partner advertised capabilities and resolve the PAUSE capabilities.

Table 15 : Pause Encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

Table 16 : Pause Resolution

Local Device		Link Partner		Local device resolution	Link partner resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR		
0	0	Don't care	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE Transmit Disable PAUSE Receive	Enable PAUSE Receive Disable PAUSE Transmit
1	0	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don't care	1	Don't care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE Receive Disable PAUSE Transmit	Enable PAUSE Transmit Disable PAUSE Receive

1.13.11 Media Independent Interface (MII)

The 78Q8430 supports an exposed MII when operating in MAC MII Mode. The MII on the 78Q8430 provides for independent transmit and receive paths for both 10 Mb/s and 100 Mb/s data rates, as described in Clause 22 of the IEEE 802.3 standard. In addition, the MII is capable of supporting HPNA-1 and -2 and other MII-based PHYs.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN, TXD[3:0], and TX_ER signals from the MAC to the external PHY. TXD[3:0] is captured on the rising edge of TX_CLK when TX_EN is asserted. TX_ER is also captured on the rising edge of TX_CLK and is asserted by the MAC to request that an error code group be transmitted.

The receive clock, RX_CLK, provides the timing reference to transfer RX_DV, RXD[3:0], and RX_ER signals from the PHY to the MAC. RX_DV transitions synchronously with respect to RX_CLK and is asserted when the PHY is presenting valid data on RXD[3:0]. RX_ER is asserted when a code group violation has been detected in the current receive packet and is also synchronous to RX_CLK.

1.13.12 Station Management Interface (SMI)

The 78Q8430 supports an exposed Station Management Interface when operating in MAC MII Mode. This interface is designed to be connected to an external PHY. Station Management registers in the external PHY are accessed with the register interface provided by the MAC.

The station management interface consists of circuitry which implements the serial protocol as described in Clause 22.2.4.4 of IEEE-802.3. A 16-bit shift register receives serial data applied to the MDIO pin at the rising edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of frame sequence and a read or write opcode, followed by the PHYAD and REGAD fields. For a read operation, the MDIO port becomes enabled as an output and the register data is loaded into a shift register for transmission. The 78Q8430 PHY can work with a one bit preamble rather than the 32 bits proscribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q8430 PHYAD indicated by the PHYAD pins, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received. Writes to registers not supported by the 78Q8430 PHY are ignored. In normal operating mode, the internal PHY responds only to a hard-wired PHY address of 00001.

1.13.13 LED Indicators

There are two LED pins that can be used to indicate various states of operation of the 78Q8430 PHY. There is an LED pin that indicates the link is up (LED0), the other LED indicates there is either RX or TX activity (LED1). In either mission mode or the external phy mode, there is no direct hardware for controlling the MAC from the PHY LED status, therefore software drivers must obtain the DUPLEX and SPEED parameters from the PHY, and configure the MAC accordingly.

1.13.14 PHY Interrupts

The 78Q8430 PHY has an Interrupt signal that is asserted whenever any of the eight interrupt bits of MR17.7:0 are set. The IntPHY bit (19) in the Interrupt Source Register (address 24h) is set to indicate an interrupt from the PHY. Individual PHY interrupt conditions can be enabled via MR17, bits 15:8, the PHY Interrupt Enable bits. PHY interrupt bits are cleared when MR17 is read.

1.14 Clock Sources

1.14.1 EMI System Clock Source

The 78Q8430 must use the external clock as the source for the EMI interface if the chip is in synchronous bus mode (BUSMODE=0). Clock frequencies of up to 50 MHz are supported in this mode. The 78Q8430 can use either the external clock, or an internal clock for the EMI interface if the chip is in asynchronous bus mode (BUSMODE=1). Clock frequencies of up to 100 MHz are supported in the external clock mode. When the internal clock is used (PHYTEST=1), a fixed 100 MHz frequency is derived from the 25 MHz PHY clock source.

1.14.2 PHY Clock Source

The 78Q8430 will use the on-chip crystal oscillator as the clock source for the PHY, if an external crystal is used. In this mode a 25 MHz crystal is connected between the XTLP and XLTN pins. Alternatively, an external 25 MHz clock source can be connected directly to the XLTP pin to supply the reference clock. In this mode of operation, a crystal is not required and the XLTN pin must be tied low. The chip senses the level of the XLTN pin, and will automatically configure itself to use the appropriate clock source.

1.14.3 Transmit Clock Generation

The transmitter uses an on-chip frequency synthesizer to generate the transmit clock. In 100BASE-TX operation, the synthesizer multiplies a 25 MHz reference clock by 5 to obtain the internal 125 MHz serial transmit clock. In 10BASE-T mode, it generates an internal 20 MHz transmit clock by multiplying a 25 MHz reference clock by 4/5. The synthesizer references either the local 25 MHz crystal oscillator, or the externally applied clock, depending on the selected mode of operation.

1.14.4 Receive Signal Qualification

The integrated signal qualifier has separate squelch and unsquelch thresholds, and includes built-in time qualifiers to ensure reliable signal detection and line noise rejection. Upon detection of two or more valid 10BASE-T or 100BASE-TX pulses on the line receive port, signal detection is indicated, and the signal detect threshold is lowered by about 40%. At this time, all adaptive circuits are released from their initial states and allowed to lock onto incoming receive data. In 100BASE-TX operation, signal detect is asserted when there is non-10Base-T signal activity detected on the line input. Signal detect will be de-asserted when no signal is received for a period of about 1.2 μ s. In 10BASE-T operation, signal detect will be asserted only while Manchester frame data is being received. In either case, the signal detect threshold will return to the squelched level whenever signal detect indication is de-asserted. Signal detect is also used to control the operation of clock/data recovery circuits to assure fast data acquisition.

1.14.5 Receive Clock Recovery

In 100BASE-TX mode, the 125 MHz receive clock is extracted using a digital DLL-based loop. When no receive signal is present, the CDR is directed to lock onto the 125 MHz transmit serial clock. When pass is asserted, the CDR will use the received MLT-3 signal as the clock reference. The recovered clock is used to re-time the data signal and for conversion of the data to NRZ format.

In 10BASE-T mode, the 20 MHz receive clock is recovered digitally from the Manchester data using a DLL locked to the reference clock. For fast acquisition, the receive PLL is locked onto the transmit reference clock during idle receive periods. When Manchester-coded preambles are detected, the CDR immediately re-aligns the phase of its clock to synchronize with the incoming Manchester data. Hence clock acquisition is immediate.

1.14.6 Exposed MII Clocks

When the internal PHY is disabled and the MAC is operating with the exposed MII connected to an external PHY, the MII transmit clock and MII receive clock are provided as inputs from the external PHY. The clocks will be operating at 25 MHz, or 2.5 MHz, depending on the network operating speed.

1.15 System Timing Summary

1.16 Reset Behavior

Reset Mode: When RESETZ is pulled low, all digital activity in the chip stops. The exceptions are the oscillator and RTC module which continue to run.

Upon negation, the software drivers are responsible to check for the presence of a serial ROM, and if present, to read in the station address, and other configuration parameters. There are three other ways that reset may be invoked: (i) internal power-on reset acts the same as H/W reset. (ii) software reset using the MAC_Ctl register, bit 2, resets the EMI bus, DMA, and MAC state machines, but does not affect the PHY. (iii) software reset using PHY reset register, MR0.15, resets the PHY, but does not affect the MAC, DMA, and EMI state machines.

1.17 Scan Test

The part contains 8 scan chains.

Table 17 : Scan Chain Definitions

Scan Chain Number	Input Pin	Output Pin	Scan clock
1	ADDR9	PROMCS	NC16
2	ADDR8	PROMDO	NC13
3	ADDR7	NC10	CSB
4	ADDR6	NC11	BUSCLK
5	ADDR5	NC17	BUSCLK
6	ADDR4	NC18	BUSCLK
7	ADDR3	NC14	BUSCLK
8	ADDR2	NC12	BUSCLK

2 REGISTER DESCRIPTIONS

2.1 Register Overview

When the device's ADDRHI pin is a "1", the register address space is selected, and a specific register is selected by a decode of the chip's lower address bits (14 to 2). For the purpose of this document the register address space values are assigned as if the ADDRHI pin was connected to the host CPU address bit 15. This produces a 64 Kbyte address space for the device, with the lower 32 Kbytes (0000h through 7FFFh) the device's memory space, and the upper 32 Kbytes (8000h through FFFFh) the device's register space.

Bits in the register tables that are blank are reserved, and will read as a "0", and are only expected to be written with a "0".

The registers of the 78Q8430 are divided into several functional groups:

- ❑ EMI Configuration Registers.
- ❑ DMA and MAC Control and Status Registers.
- ❑ PHY Management Registers.

In normal operation, once setup is complete, most registers do not need to be accessed directly. Transmit and receive operations are done using continuous cyclic queues, or rings. Control and status information is communicated through data structures. DMA control registers need to be accessed at initialization time, in order to initiate operation. MAC registers may need to be accessed for special configuration needs, such as setting the ARC to do address filtering. For interrupt based drivers, some of the DMA and MAC registers are accessed in the interrupt handler, to enable and disable interrupts, to determine the cause of an interrupt, and to clear interrupt condition bits. Flow control registers may be accessed by drivers to monitor the progress of local and remote PAUSE commands. Network Management registers need to be accessed for initialization and periodic reporting, if the H/W Network Management block is used to support managed network applications.

There are two basic types of register access:

- ❑ RO - Read Only. Writing to a RO register has no effect.
- ❑ R/W - Read and Write. The user can read and write the register. The controller may also write the register, and some parts may be reserved, read only, or have special semantics. So the user may not always be able to read what was written.

The registers with access marked with "*" have special semantics, such as bits which are "write 1 to clear", "self-clearing", "sticky", etc. as explained in the detailed register descriptions. Reserved bits are initialized to 0. Software should read them as "don't care" and leave them unchanged when writing to registers, to aid in compatibility with future uses. Software should not depend on the value of reserved fields being 0.

2.2 DMA Control and Status Registers

2.2.1 DMA Register Overview

There are three queues which are jointly managed by the DMA engine and the system software: the Transmit Queue, the Receive Queue, and the free Buffer List. The transmit queue is a list of frame descriptors which are ready for transmission. The receive queue is a list of frame descriptors which have been received and are ready for processing by the system software. The buffer list is a list of buffer descriptors which describes areas of system memory that can be used to store received data. The free descriptor area (FDA) is the memory area where the controller writes the frame descriptors and buffer descriptors for the Receive Queue.

Table 18 shows the register name, symbol, address, size, and access type for each DMA control register. These registers provide support for a transmit queue, a receive queue, free buffer list, and a free descriptor area. Some registers control fragmentation sizes or polling rates. Some registers provide support for receiving, processing, and generating Full Duplex PAUSE Operations and other forms of MAC Control packets.

Table 18 : DMA Register Group

NAME	SYMBOL	ADDR	BYTES	ACCESS
DMA Control	DMA_Ctl	8000h	4	R/W
Transmit Frame Pointer	TxFrmPtr	8004h	4	R/W
Transmit Threshold	TxThrsh	8008h	2	R/W
Transmit Polling Counter	TxPollCtr	800Ch	2	R/W
Buffer List Frame Pointer	BLFrmPtr	8010h	4	R/W
Interrupt Delay Counter	IntDlyCnt	8014h	4	R/W
Interrupt Enable	Int_En	8018h	2	R/W
Free Descriptor Area Base	FDA_Bas	801Ch	4	R/W
Free Descriptor Area Limit	FDA_Lim	8020h	2	R/W
Interrupt Source	Int_Src	8024h	3	R/W*
Pause Count	PauseCnt	8030h	2	RO
Remote Pause Count	RemPauCnt	8034h	2	RO
Transmit Control Frame Status	TxConFrmStat	8038h	2	R/W

2.2.2 DMA Control Register, "DMA_Ctl", 8000h

31	30	29	28	27	26	25	24
						RMemBank	RmSwReq
23	22	21	20	19	18	17	16
RxAlign		RmRxInit	RmTxInit		IntMask	SWIntReq	TxWakeUp
15	14	13	12	11	10	9	8
RxBigE	TxBigE	TestMode					DmBurst8
7	6	5	4	3	2	1	0
DmBurst[7:4]				DmBurst[3:2]			

DmBurst[8:2]	Dma Burst Size	R/W. Not affected by software reset. Size of data bursts (in Dwords) between on-chip buffer memory and the transmit and receive hardware. This value will affect buffer access latency that the CPU experiences when transmit and receive are active.
TestMode	Test Mode	R/W. Not affected by software reset. Reserved.
TxBigE	Transmit Big Endian	R/W. Not affected by software reset. When set, treat all transmit data as big endian.
RxBigE	Receive Big Endian	R/W. Not affected by software reset. When set, treat all receive data as big endian.
TxWakeUp	Transmit Wake Up	R/W/SC. Not affected by software reset. Writing a "1" aborts the current transmit polling cycle and begins transmit operation. Writing a "0" has no affect. Self clears when transmit hardware begins operation.
SWIntReq	Software Intr. Request	R/W. Not affected by software reset. Writing a "1" will cause a software interrupt to be generated. Writing a "0" has no affect.
IntMask	Interrupt Mask	R/W. Not affected by software reset. Writing a "1" disables interrupt generation from the chip. Writing a "0" enables interrupt generation from the chip.
RmTxInit	RMON Tx Initialize	R/W/SC. Not affected by software reset. Writing a "1" causes the Transmit RMON counters and clear registers to be initialized. Writing a "0" has no affect. Self clears when RMON operation completed.
RmRxInit	RMON Rx Initialize	R/W/SC. Not affected by software reset. Writing a "1" causes the Receive RMON counters and clear registers to be initialized. Writing a "0" has no affect. Self clears when RMON operation completed.

RxAlign	Receive Alignment	R/W. Initialized to '00' by either hardware or software reset. Controls alignment of received packets in the buffer memory. 00 - (default) no bytes are skipped, 4-byte alignment. 01 - offset by 1 byte in first data buffer. 10 - offset by 2 bytes in first data buffer. 11 - offset by 3 bytes in first data buffer.
RMSwRq	RMON Switch Request	R/W/SC. Not affected by software reset. Writing a "1" initiates a switch in ownership of the two internal RMON memory banks. Self clears when memory switch is completed.
RMemBank	RMON Memory Bank Select	R/O. Initialized to '0' by either hardware or software reset. When 0, software can access bank 1, RMON controls bank 0. When 1, software can access bank 0, RMON controls bank 1

Hardware reset to value 0000_0020h. (The low order byte 20h indicates a DmBurst default of 32 bytes)

The DMA control register controls the transfer of data between the transmit and receive engines and the buffer memory, burst size, endian byte ordering, and test mode functionality. It also controls a number of other DMA functions, such as wake-up on transmit and software interrupt.

The DmBurst field controls the size of data transfers requested across the internal bus when transferring data between the buffer ram and the transfer hardware. It is a nine-bit register, with the two low-order bits forced to zero, (i.e. burst transfer sizes must be a multiple of 4-bytes). The default value after hardware reset is 32 bytes or 8 double words. This can be modified by the software driver. DmBurst field cannot be set to zero; an attempt to write a zero burst transfer size is ignored.

The Transmit and Receive Big Endian bits support the transmission and reception of data which has been ordered for a 32-bit Big Endian machine. Note that only data (bytes in the areas pointed to by the buffer descriptors) are affected. Control information, which includes registers, frame descriptors, and buffer descriptors, are always in native EMI bus, or little endian format.

The Transmit Wake Up bit supports immediate transmission of data, rather than waiting for the current polling cycle to end. If set, and if the transmitter is polling, the current polling cycle will be terminated. This bit is cleared at the end of the current polling cycle. Writing zero has no effect.

Software interrupt is provided by the controller as a service for software drivers.

Interrupt mask disables the chip interrupt, if the software driver does not want to be interrupted while processing the cause of the chip interrupt. The Interrupt Delay Register also controls the interrupt.

The RMON Transmit and Receive Initialize registers are used to control default initialization of the RMON counters and clear values. Writing a 1 causes initialization to begin. Writing a 0 has no effect. Once the initialization is complete, the bit will be cleared. Initialization of the RMON counters and memory takes about 128 BUSCLK cycles.

2.2.3 Transmit Frame Pointer, “TxFrmPtr”, 8004h

31	30	29	28	27	26	25	24
TxFrmPtr[31:24]							
23	22	21	20	19	18	17	16
TxFrmPtr[23:16]							
15	14	13	12	11	10	9	8
TxFrmPtr[15:8]							
7	6	5	4	3	2	1	0
TxFrmPtr[7:4]							EOL

EOL	End of List	R/W. When set to “1”, the address is invalid for use by the controller. The controller will wait for system software to clear the bit to “0”, before proceeding to use the frame descriptor pointed to by “TxFrmPtr”.
TxFrmPtr	Transmit Frame Pointer	R/W. Address pointer to the first receive queue frame descriptor.

Reset to value 0000_0001h by either hardware or software reset.

The transmit frame pointer contains the address of the first frame descriptor to read for the transmit queue. The system must set the pointer field to a properly initialized frame descriptor, and clear the EOL bit to enable transmission. Clearing the “EOL” bit during initialization starts the transmit queue “gather” engine. A valid address must be aligned to a 16 byte boundary (i.e. bits [3:0] must be zero). After the “gather” engine begins operation this register should not be written, as it is under control of the hardware.

As the hardware completes use of the current transmit queue frame descriptor at the end of a packet transmission, it will check the “EOL” bit, to determine if it can proceed to the “NEXTFD”. If the “EOL” bit is “0” the hardware will copy the value of the “NEXTFD” field into this pointer, and begin to process the next transmit queue packet. Otherwise the hardware will again wait for software to clear the “EOL” bit to “0” before proceeding with the next transmit task.

2.2.4 Transmit Threshold Control Register, “TxThrsh”, 8008h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
					TxThrsh[10:8]		
7	6	5	4	3	2	1	0
TxThrsh[7:0]							

TxThrsh	Transmit Threshold	R/W. The value is held in the internal parameter / staging RAM, so hardware and software resets have no effect. Sets the minimum number of bytes that must be available in the transmit FIFO before a MAC transmit operation is started.
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The transmit threshold register controls the buffer latency for transmitting packets. If the threshold value is non-zero, then data transfer to the MAC will begin as soon as the DMA transmit FIFO contains this number of bytes, or as soon as a complete packet is in the FIFO. If the threshold value is zero, data transfer to the MAC starts immediately.

If the threshold value is set too low, the DMA transmit FIFO may underrun due to EMI bus latency. If this occurs, as indicated by the MAC transmit status, system software should increase the TxThold value.

Care should be taken not to set the threshold value greater than 1620 decimal when in long packet mode. This may cause buffer memory to fill without enabling transmission, causing the transmitter to hang.

2.2.5 Transmit Polling Control Register, "TxPollCtr", 800Ch

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
				TxPollCtr[11:8]			
7	6	5	4	3	2	1	0
TxThrsh[7:0]							

The value is held in the internal parameter / staging RAM, so hardware and software resets have no effect.

The transmit polling counter controls the frequency with which the controller polls for packets to transmit. If the value is zero, polling is not performed. Otherwise, an internal counter will be set to this value, and decrements to zero. When the register reaches zero, a read will be done to see if a new transmit packet has arrived. With a 100 MHz clock, each unit in the polling counter is equivalent to 10 ns. The maximum polling time is $2^{11} \times 10 \text{ ns} = 20.48 \text{ micro-seconds}$. It is the responsibility of the device S/W drivers to initialize this register.

2.2.6 Buffer List Frame Pointer, “BLFrmPtr”, 8010h

31	30	29	28	27	26	25	24
BLFrmPtr[31:24]							
23	22	21	20	19	18	17	16
BLFrmPtr[23:16]							
15	14	13	12	11	10	9	8
BLFrmPtr[15:8]							
7	6	5	4	3	2	1	0
BLFrmPtr[7:4]							EOL

EOL	End of List	R/W. When set to “1”, the address is invalid for use by the controller. The controller will wait for system software to clear the bit to “0”, before proceeding to use the frame descriptor pointed to by “BLFrmPtr”.
BLFrmPtr	Buffer List Frame Pointer	R/W. Address pointer to the first receive queue frame descriptor.

Reset to value 0000_0001h by either hardware or software reset.

The buffer list frame pointer contains the address of the first frame descriptor to read for acquiring free buffer descriptors. The system must set the pointer field to a properly initialized frame descriptor, and clear the EOL bit to enable reception. Clearing the “EOL” bit during initialization starts the receive queue “scatter” engine. A valid address must be aligned to a 16 byte boundary (i.e. bits [3:0] must be zero). After the “scatter” engine begins operation this register should not be written, as it is under control of the hardware.

As the hardware completes use of the current receive queue frame descriptor at the end of a receive packet, it will check the “EOL” bit, to determine if it can proceed to the “NEXTFD”. If the “EOL” bit is “0” the hardware will copy the value of the “NEXTFD” field into this pointer, and prepare to process the next received packet. Otherwise, the hardware will again wait for software to clear the “EOL” bit to “0” before proceeding with the next transmit task.

2.2.7 Interrupt Delay Register, “IntDlyCnt”, 8014h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IntDlyCnt[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntDlyCnt[15:0]															

IntDlyCnt	Interrupt Delay Count	R/W. Delays the next assertion of the interrupt pin.
-----------	-----------------------	--

Reset to value 0000_0000h by hardware reset.

Software reset has no effect.

The 32-bit unsigned count value is loaded into a counter and decremented to zero. The counter is decremented once each internal clock cycle.

The purpose of this register is to delay the assertion of the INTB signal, to allow for system recovery. The default delay time is 0, i.e. no delay. Other values may be programmed by the device S/W driver. The counter begins decrementing as soon as the INTB signal is de-asserted. INTB deassertion is usually caused by the S/W driver writing the IntMask bit of the DMA_Ctl register, i.e. the delay period includes processing time while the IntMask bit is set.

2.2.8 Interrupt Enable Register, “Int_En”, 8018h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
					ExtEvtEn		
15	14	13	12	11	10	9	8
		PhyIntEn	LnkChgEn		TCtlCmpEn		
7	6	5	4	3	2	1	0
EarNotEn						BLExEn	FDAExEn

FDAExEn	Free Descriptor Area Exhausted Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt if the Free Descriptor Area becomes exhausted, i.e. if the controller encounters a block in the FDA which is still owned by the system
BLExEn	Buffer List Exhausted Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt if the controller encounters a descriptor in the BL which is still owned by the system
EarNotEn	Early Notify Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt after the controller writes the first buffer and buffer descriptor of a received packet.
TCtlCmpEn	Tx Control Complete Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt when transmission of a MAC Control packet is completed.
LnkChgEn	Link Change Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt if there is a change in the link status from the PHY.
PhyIntEn	Phy Int. Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt if there is a change in the interrupt pin from the PHY. When the chip is in external PHY mode, the interrupt pin is EEVNT1.
ExtEvtEn	External Event Enable	R/W. Not affected by software reset. Writing a “1” enables an interrupt if either of the external interrupt pins (EEVNT1 or EEVNT2) become asserted.

Reset to value 0000_0000h by hardware reset.

The interrupt enable register controls the generation of interrupts in response to errors and other conditions detected by the 78Q8430. The Early Notify enable bit supports applications which want to minimize latency. Note that the Frame Descriptor will not be valid when the Early Notify is processed. Only the first buffer descriptor is valid when this interrupt is signalled.

2.2.9 Free Descriptor Area Base Register, “FDA_Bas”, 801Ch

31	30	29	28	27	26	25	24
FDA_Bas[31:24]							
23	22	21	20	19	18	17	16
FDA_Bas[23:16]							
15	14	13	12	11	10	9	8
FDA_Bas[15:8]							
7	6	5	4	3	2	1	0
FDA_Bas[7:4]							

FDA_Bas	FDA Base Address	R/W. Address pointer to the first receive queue frame descriptor.
---------	------------------	---

Hardware reset to value 0000_0000h

Software reset has no effect.

The Free Descriptor Area base register contains the starting address of the area reserved for the controller to write frame and buffer descriptors for received packets. The address is 16 byte aligned (i.e. bits [3:0] are always zero).

2.2.10 Free Descriptor Area Limit Register, “FDA_Lim”, 8020h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
FDA_Lim[15:8]							
7	6	5	4	3	2	1	0
FDA_Lim[7:4]							

FDA_Lim	FDA Limit	R/W. Contains the number of 16 byte frame descriptors allocated in the FDA.
---------	-----------	---

Hardware reset to value 0000_0000h

Software reset has no effect.

The Free Descriptor Area limit register contains the count of the number of 16-byte blocks in the receive descriptor area. The address is 16 byte aligned (i.e. bits [3:0] are always zero). Alternatively, the low 16 bits can be viewed as a byte offset from the Free Descriptor Area Base register. Each 16-byte block holds one frame descriptor, or two eight-byte buffer descriptors. So the maximum size of a single descriptor area is (4095 * 16) or 64K bytes - 16 bytes. The “FDA_Lim” register must point to the lowest offset in the FDA where a new frame descriptor can safely begin (i.e. enough space must be allowed for the maximum size packet to have enough space for a maximum number of buffer descriptors to be written).

2.2.11 Interrupt Source Register, "Int_Src", 8024h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
				PHYInt	ExtEvtInt	RMONInt	ExDefInt
15	14	13	12	11	10	9	8
LnkChgInt			BLEx	FDAEx		TxCtlCmp	BDOORInt
7	6	5	4	3	2	1	0
	EarNotInt	SWInt	BLExInt	FdaExInt		MacRxInt	MacTxInt

MacTxInt	MAC Transmit Interrupt	R/W1Clr. Set when MAC transmit engine writes the packet's ending transmit status to the frame descriptor memory, and any of the transmit interrupt conditions are set.
MacRxInt	MAC Receive Interrupt	R/W1Clr. Set when MAC receive engine writes the packet's ending receive status to the frame descriptor memory, and the status has the receive interrupt bit set.
FdaExInt	Free Descriptor Area Exhausted Interrupt	RO. Set when FDAEx bit in this register is set, and FDAExEn in the interrupt enable register is set. Cleared when FDAEx bit is serviced.
BLExInt	Buffer List Exhausted Interrupt	RO. Set when BLEx bit in this register is set, and BLExEn in the interrupt enable register is set. Cleared when BLEx bit is serviced.
SWInt	Software Interrupt	RO. Set when Software Interrupt Request (DMACTL[17]) bit is set.
EarNotInt	Early Notify Interrupt	R/W1Clr. Set when the controller writes the first buffer and buffer descriptor of a received packet, and the EarNotEn (INTEN[7]) bit is set.
BDOORInt	Buffer Descriptor Out Of Range Interrupt	R/W1Clr. Set when the controller detects the buffer descriptor index is out of range (more than 28). This chip only allows a frame descriptor to divide a packet into a maximum of 28 buffer fragments.
TxCtlCmp	Transmit Control Complete	R/W1Clr. Set when the MAC completes the transmit of a control packet, and the TxCtlCmpEn (INTEN[10]) bit is set.
FDAEx	Free Descriptor Area Exhausted	R/W1Clr. Set when the Free Descriptor Area is exhausted (all receive frame descriptors belong to the host software driver).
BLEx	Buffer List Exhausted	R/W1Clr. Set when the Buffer List Area is exhausted (all buffer list descriptors belong to the host software driver).

LnkChgInt	Link Change Interrupt	R/O. Interrupt caused by a change in Link Status. Cleared by writing one to the Link Changed bit (LnkChg, bit 8) of the MACCTL register.
ExDefInt	Excessive Deferral Interrupt	R/W1Clr. Set when the controller detects excessive MAC transmit deferrals, and the EnExDefer (TXCTL[9]) bit is set.
RMONInt	RMON Interrupt	R/O. Set when a RMON counter rolls over.
ExtEvtInt	External Event Interrupt	R/W1Clr. Set when an External Event is detected.
PHYInt	PHY Interrupt	R/O. Set when the PHY Interrupt pin changes state. Cleared by clearing MR17.

Reset to value 0000_0000h by either hardware or software reset.

The Interrupt Source Register is read by system software, to see if there is an interrupt associated with the Ethernet controller. In addition, the register provides status bits for some conditions which are not reported elsewhere. If bits 15 and 10 through 0 are all zeroes, the controller did not generate an interrupt. If an interrupt is associated with the Ethernet controller, all further interrupts from the Ethernet controller can be masked with the IntMask bit of the DMA Control register.

Bit 8 is set if a single Frame Descriptor requires more than 28 Buffer Descriptors. Bit 13 is set whenever a DMA RAM parity error is detected. Bit 7 is set and an interrupt is generated, only if the DParErrEn bit of the Interrupt Enable Register is set.

S/W drivers should clear the IntMACTx or IntMACRx bits before processing as many Tx and Rx completed frames as possible. S/W should be written to anticipate that there might be zero completed frames for an interrupt, because the frame causing the interrupt was processed as part of the previous interrupt.

2.2.12 Pause Count Register, "PauseCnt", 8030h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PauseCnt[15:0]															

PauseCnt	Received Pause Count	R/W. Count of time slots that Transmitter is being paused by receiving a MAC Control PAUSE operation packet.
----------	----------------------------	--

Reset to value 0000_0000h by either hardware or software reset.

The pause count register provides the current value of the received pause counter. A value of 0 indicates the MAC is not paused.

Each unit is one slot time, or 512 bit times. For 10BASE-T, a bit time is 100ns; a counter unit is 51.2 micro-seconds. For 100BASE-TX, a bit time is 10ns; a counter unit is 5.12 micro-seconds.

2.2.13 Remote Pause Count Register, “RemPauCnt”, 8034h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RemPauCnt[15:0]															

RemPauCnt	Remote Pause Count	R/W. Count of time slots that the remote MAC is being paused by sending a PAUSE operation packet.
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Reset to value 0000_0000h by either hardware or software reset.

The remote pause count register provides an approximate current value of the remote pause counter, based on when a PAUSE command was sent.

Each unit is one slot time, or 512 bit times. For 10BASE-T, a bit time is 100ns; a counter unit is 51.2 micro-seconds. For 100BASE-TX, a bit time is 10ns; a counter unit is 5.12 micro-seconds.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								TxCtlFRmStat[22:16]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxCtlFRmStat[15:0]															

TxCtlFrmStat	Transmit Control Frame Status	R/W. Duplicate information with the Transmit Status Register, Tx_Stat, 804Ch.
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The Transmit Control Frame Status provides the status of sending a MAC Control packet to a remote station via the SdPause bit of the Transmit Control register. When the transmission is complete, the software drivers may pick up the status from this register. Software can reset this register by clearing it before initiating the transfer of a MAC Control frame. The TxCtlCmpEn bit of the Interrupt Enable register provides for an option to generate an interrupt on completion of MAC Control packet transmission.

For bit field definitions, see the MAC Tx stat register description.

2.3 MAC Control and Status Registers

2.3.1 MAC Register Overview

The DMA and MAC control and status registers are broken into several groups.

- ❑ Flow Control Registers.
- ❑ MAC Control and Status Registers.
- ❑ Network Statistics Access and Control Registers.
- ❑ Wake Up Services Control and Status Registers.

Table 19 shows the functional group, register name, symbol, address, size, and access type for each MAC control and status register. These registers are generally loaded from an EEPROM or ROM on chip power up or chip reset. Some of these registers, such as the ARC control and error count registers, are accessed by system software drivers while the MAC is active. The MAC transmit and receive control and status registers are generally controlled by the DMA engine after they are setup.

Table 19 : MAC Register Group

NAME	SYMBOL	ADDR	BYTES	ACCESS
MAC Control	MAC_Ctl	8040h	2	R/W*
ARC Control	ARC_Ctl	8044h	1	R/W
Transmit Control	Tx_Ctl	8048h	2	R/W
Transmit Status	Tx_Stat	804Ch	3	R/O
Receive Control	Rx_Ctl	8050h	2	R/W
Receive Status	Rx_Stat	8054h	4	R/O
Station Management Data	MD_Data	8058h	2	R/W
Station Management Control and Address	MD_CA	805Ch	2	R/W*
ARC Address	ARC_Adr	8060h	2	R/W
ARC Data	ARC_Data	8064h	4	R/W
ARC Enable	ARC_Ena	8068h	3	R/W
PROM Control	PROM_Ctl	806Ch	2	R/W*
PROM Data	PROM_Data	8070h	2	R/W
Missed Error Count	Miss_Cnt	8074h	2	R/W*

Table 20 shows the register name, symbol, address, size, and access type for each Network Statistics access and control registers and the IP Check Sum Control register.

Table 20: Network Statistics and IP Checksum Registers

Name	Symbol	Addr	Bytes	Access
Count Data Register	CntData	80h	4	R/W
Count Access Register	CntAcc	84h	4	R/W
Transmit RMON Interrupt Enable	TxRmlntEn	88h	4	R/W
Receive RMON Interrupt Enable	RxRmlntEn	8Ch	4	R/W
IP Check Sum Control Register	IPChkCtl	90h	2	R/W

Table 21 shows the register name, symbol, address, size, and access type for each Wake Up Control control and status register.

Table 21: Wakeup Control and Status Registers

Name	Symbol	Addr	Bytes	Access
Wake Up Control Register	WU_Ctl	A0h	4	R/W
Wake Up Status Register	WU_Stat	A4h	4	R/O
OnNow Result Register 0	ON_Res0	A8h	4	R/W
OnNow Result Register 1	ON_Res1	ACh	4	R/W
OnNow Result Register 2	ON_Res2	B0h	4	R/W
OnNow Result Register 3	ON_Res3	B4h	4	R/W
OnNow Result Register 4	ON_Res4	B8h	4	R/W
Host Not Responding Initial Count Register	HNR_CNT	BCh	4	R/W

2.3.2 MAC Control Register, “MAC_Ctl”, 8040h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
		ENMISRL			MISROLL		LINKCHG
7	6	5	4	3	2	1	0
			MACLOOP		MACSRST	HALTIMM	HALTREQ

HALTREQ	Halt Request	R/W. Initialized to “0” by hardware reset. Not affected by software reset. Writing a “1” stops transmission and reception after completion of any current packets.
HALTIMM	Halt Immediate	R/W. Initialized to “0” by hardware reset. Not affected by software reset. Writing a “1” stops transmission and reception immediately.
MACSRST	MAC Software Reset	R/W/SC. Initialized to “0” by hardware reset. Writing a “1” resets all EMI, DMI, and MAC state machines and FIFOs. Self Clearing at the end of the software reset. Does not affect the embedded PHY.
MACLOOP	MAC Loopback	R/W. Initialized to “0” by hardware reset. Not affected by software reset. Writing a “1” causes transmit signals to be presented as input to the receiver without leaving the controller
LINKCHG	Link Changed	R/W1Clr. Initialized to “0” by hardware and software reset. Writing a “1” clears the internal generator of the Int_Link signal interrupt condition. Writing 0 has no effect
MISROLL	Missed Roll	R/O. Initialized to “0” by hardware reset. Not affected by software reset. Missed error counter rolled over (reached 8000h). Cleared by reading the Missed Count register.
ENMISRL	Enable Missed Roll	R/W. Initialized to “0” by hardware reset. Not affected by software reset. Writing a “1” enables an interrupt when missed error counter rolls over.

Reset to value 0000_0000h by hardware reset.

Software reset is invoked by setting bit 2. Bit 2 is cleared after software reset is complete. Other bits are not affected by software reset.

The MAC control register provides global control and status information for the MAC. The MissRoll bit is a status bit, all the others are control bits.

Software reset is delayed for three clock cycles, to allow normal completion of the EMI operation which writes the Reset bit. Software can use the Tx_ctl and Rx_ctl registers to request a halt after current network transactions are complete before using reset.

The Missed Roll bit is set when the counter rolls over and cleared when S/W reads the Missed Count register.

2.3.3 Address Recognition Circuit Control Register, "ARC_Ctl", 8044h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
			CompEn	NegARC	BroadAcc	GroupAcc	StationAcc

StationAcc	Station Accept	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables accepting packets with a "unicast" station address.
GroupAcc	Group Accept	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables accepting packets with a multicast-group address
BroadAcc	Broadcast Accept	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables accepting packets with a broadcast address
NegARC	Negate ARC	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "0" selects accepting packets ARC recognizes and rejecting others. Writing a "1" selects rejecting packets ARC recognizes and accepting others.
CompEn	Compare Enable	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables the ARC compare mode.

Reset to value 0000_0000h by hardware reset.

The ARC circuit recognizes three types of Ethernet addresses:

- ❑ A Station address has an even first byte, i.e. 00-00-00-00-00-00.
- ❑ The Broadcast address is defined to be ff-ff-ff-ff-ff-ff.
- ❑ A Multicast-group address has an odd first byte, (but not Broadcast) i.e. 01-00-00-00-00-00.

Setting CompEn enables the ARC to match incoming destination addresses with addresses stored in the ARC memory. Clearing CompEn forces the ARC to fail all attempts to match incoming addresses in the ARC memory. The three accept bits override ARC rejections. To reject all packets, clear all bits in ARC_ctl.

There are several ways to place the MAC in promiscuous mode, and accept all packets.

- ☐ set the ARC to accept all three types of address.
- ☐ set the Negative ARC bit, but clear the Compare Enable bit.
- ☐ set the Negative ARC bit, set the Compare Enable bit, but do not enable any ARC entries.

When ARC compare mode is enabled, the ARC memory is read for addresses to filter incoming messages. ARC entries are set and individually enabled and disabled.

2.3.4 Transmit Control Register, "Tx_Ctl", 8048h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
	EnComp	EnTxPar	EnLateColl	EnExColl	EnLCarr	EnExDefer	EnUnder
7	6	5	4	3	2	1	0
SQEEEn	SdPause	NoExDef	FstBack	NoCRC	NoPad	TxHalt	TxEn

TxEn	Transmit Enable	R/W. Initialized to "0" by either hardware or software reset. Writing a "1" enables transmission. Writing a "0" halts transmission immediately.
TxHalt	Transmit Halt Request	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" halts transmission at the completion of the current packet.
NoPad	Suppress Padding	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" disables the generation of pad bytes for packets with less than 64 bytes.
NoCRC	Suppress CRC	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" disables the generation of the CRC at the end of the packet.
Fstback	Fast Back-off	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" uses accelerated backoff timers and byte counts (chip test mode).
NoExDef	No Excessive Deferral	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" suppresses the checking of excessive deferrals.
SdPause	Send Pause	R/W/SC. Initialized to "0" by either hardware or software reset. Writing a "1" sends a PAUSE Command or other MAC Control packet. Self clears when control packet completed.
SQEEEn	SQE Enable	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables SQE checking.
EnUnder	Enable Underrun	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables generation of an interrupt if the transmit fifo underruns.
EnExDefer	Enable Excessive Deferral	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables generation of an interrupt if the MAC transmission is deferred for 242.88 us in 100 Mb mode, or 2.4288 ms in 10 Mb mode.

EnLCarr	Enable Lost Carrier	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables an interrupt if carrier sense is not detected or lost during the transmission of a packet.
EnExColl	Enable Excessive Collision	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables an interrupt if 16 collisions occur in the same packet.
EnLateColl	Enable Late Collision	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables an interrupt if a collision occurs within 512 bit times (64 bytes).
EnTxPar	Enable Transmit Parity	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables an interrupt if the MAC transmit FIFO has a parity error.
EnComp	Enable Completion	R/W. Initialized to "0" by hardware reset. Not affected by software reset. Writing a "1" enables an interrupt when the MAC transmits or discards one packet.

Reset to value 0000_0000h by hardware reset.

The Fast Back-off bit should not be set during normal operation. To receive an interrupt after each packet, set the enable completion and all the MAC error enable bits. Interrupts may also be enabled only for specific conditions. SQE checking is controlled by the PHY operating mode.

2.3.5 Transmit Status Register, “Tx_Stat”, 804Ch

31	30	29	28	27	26	25	24
							TxTUErr
23	22	21	20	19	18	17	16
TxIPErr	TxHNR	TxPAUSE	TxMACC	TxVLAN	TxBCast	TxMCast	SQErr
15	14	13	12	11	10	9	8
TxHalted	Comp	TxPar	LateColl		LCarr	ExDefer	Under
7	6	5	4	3	2	1	0
IntTx	Paused	TxDefer	ExColl	TxColl			

TxColl	Transmit Collision Count	R/W. Count of the collisions in transmitting the current packet.
ExColl	Excessive Collision	R/W. Set if 16 collisions occur in the same packet (packet skipped).
TxDefer	Transmit Deferred	R/W. Packet was delayed because of deferral during transmission.
Paused	Transmitter Paused	R/W. Set if transmission was paused after completion of the current packet.
IntTx	Interrupt on Transmit	R/W. Set if transmission of packet caused an interrupt condition.
Under	Underrun	R/W. MAC transmit FIFO underrun condition detected during transmission.
ExDefer	Excessive Deferral	R/W. MAC transmission deferred for more than MAX_DEFERRAL time.
LCarr	Lost Carrier	R/W. No carrier sense detected or carrier dropped during transmission.
LateColl	Late Collision	R/W. A collision occurred after 512 bit times (64 byte times).
TxPar	Transmit Parity Error	R/W. MAC transmit FIFO detected a parity error.
Comp	Completion	R/W. MAC transmitted or discarded one packet.
TxHalted	Transmission Halted	R/W. Transmission was halted by clearing TxEn or setting TxHalt.
SQErr	Signal Quality Error	R/W. No heart beat signal observed at end of transmission.
TxMCast	Multi-cast Transmit	R/W. Set if MAC transmitted a Multi-cast Packet.

TxBCast	Broadcast Transmit	R/W. Set if MAC transmitted a Broadcast Packet.
TxVLAN	VLAN tagged Transmit	R/W. Set if MAC transmitted a VLAN tagged Packet.
TxMACC	MAC Control Transmit	R/W. Set if MAC transmitted a MAC Control Packet.
TxPAUSE	PAUSE Transmit	R/W. Set if MAC transmitted a MAC Control PAUSE packet.
TxHNR	Tx Host Not Responding	R/W. Set if Host Not Responding packet was transmitted before this packet.
TxIPErr	Tx IP Checksum Error	R/W. Set if IP checksum insertion is not enabled, an IP packet is detected, and the calculated IP Checksum does not match detected IP Checksum.
TxTUErr	Tx TCP/UDP Error	R/W. Set if TCP or UDP checksum insertion is not enabled, and a detected checksum does not match the calculated checksum.

Reset to value 0000_0000h by hardware or software reset.

Register is cleared at beginning of each packet transmitted. The transmission status flags are set whenever the corresponding event occurs. In addition, an interrupt is generated if the corresponding enable bit in the transmit control register is set.

The low order five bits can be read and masked as a single collision count, i.e when ExColl is 1, TxColl is 0. If TxColl is non-zero, then ExColl is 0. MAX_DEFERRAL time is 0.24288 ms for 100-Mbit/s, 2.42880 ms for 10-Mbit/s. If TxMCast and TxBCast (bits 17:18) are both 0, then a Unicast Packet was transmitted.

2.3.6 Receive Control Register, “Rx_Ctl”, 8050h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
	EnGood	EnRxPar	EnLengthEr	EnLongEr	EnOver	EnCRCErr	EnAlign
7	6	5	4	3	2	1	0
IgnorLerr	IgnorCRC	PassCtl	StripCRC	ShortEn	LongEn	RxHalt	RxEn

RxEn	Receive Enable	R/W. Writing a “1” enables receiver. Writing a “0” stops the receiver immediately.
RxHalt	Receive Halt Request	R/W. Writing a “1” enables halts the receiver after the reception of any current packet.
LongEn	Long Enable	R/W. Writing a “1” enables good frames longer than 1518 bytes (1522 bytes for VLAN)
ShortEn	Short Enable	R/W. Writing a “1” enables reception of frames shorter than 64 bytes
StripCRC	Strip CRC Value	R/W. Writing a “1” enables check the receive CRC, but strip it from the message.
PassCtl	Pass Control Packets	R/W. Writing a “1” enables passing of received MAC Control packets to system
IgnorCRC	Ignore CRC Value	R/W. Writing a “1” disables checking the receive CRC
IgnorLErr	Ignore Length Error	R/W. Writing a “1” disables checking for length errors
EnAlign	Enable Alignment	R/W. Writing a “1” enables an interrupt upon receipt of a packet whose length in bits is not a multiple of eight, and whose CRC is invalid
EnCRCErr	Enable CRC Error	R/W. Writing a “1” enables an interrupt upon receipt of a packet whose CRC is invalid or during its reception, the PHY asserts Rx_er
EnOver	Enable Overflow	R/W. Writing a “1” enables an interrupt upon receipt of a byte when the MAC receive FIFO is full
EnLongErr	Enable Long Error	R/W. Writing a “1” enables an interrupt upon receipt of a frame longer than 1518 bytes (1522 bytes for VLAN), unless the long enable bit is set

EnLenErr	Enable Length Error	R/W. Writing a “1” enables an interrupt upon receipt of a frame with out-of-range length error.
EnRxPar	Enable Receive Parity	R/W. Writing a “1” enables an interrupt if MAC receive FIFO detects a parity error
EnGood	Enable Good	R/W. Writing a “1” enables an interrupt upon receipt of a packet with no errors

Hardware reset to value 0000_0000h.

Software reset clears RxEn and does not affect other values.

To receive an interrupt after each packet, set the good enable and all the error enable bits. Interrupts may also be enabled only for specific conditions.

The frame lengths above do not include preamble and Start Frame Delimiter (SFD).

2.3.7 Receive Status Register, "Rx_Stat", 8054h

31	30	29	28	27	26	25	24
RxTUErr	RxIPErr	ArcEntry[4:0]				ArcStat[3]	
23	22	21	20	19	18	17	16
ArcStat[2:0]			RxPause	RxVlan	RxBCast	RxMCast	
15	14	13	12	11	10	9	8
RxHalted	Good	RxPar	TypFrm	LongErr	Overflow	CRCErr	AlignErr
7	6	5	4	3	2	1	0
	IntRx	CtlRcvd	LenErr				

LenErr	Length Error	R/W. Length field did not match packet size. Not set for type values out of range, and packets with length field less than 46 and length of 64.
CtlRcvd	Control Frame Received	R/W. Set if packet received is a MAC Control Frame, i.e. type = 8808h, and ARC recognizes address
IntRx	Interrupt on Receive	R/W. Set if reception of packet caused an interrupt condition. This includes Good Received, if the EnGood bit is set.
AlignErr	Alignment Error	R/W. Frame length in bits was not a multiple of eight and the CRC was invalid.
CRCErr	CRC Error	R/W. CRC at end of packet did not match computed value, or the PHY asserted Rx_er during packet reception.
Overflow	Overflow Error	R/W. The MAC receive FIFO was full, a received byte was lost.
LongErr	Long Error	R/W. Received a frame longer than 1518 bytes (1522 if a VLAN). Not set if the long enable bit in Rx_Ctl is set.
TypFrm	Type Frame	R/W. Set if length field is out-of-range, i.e. a type field.
RxPar	Receive Parity Error	R/W. The MAC receive FIFO has detected a parity error.
Good	Good Received	R/W. Successfully received a packet with no errors, including type frames where the Type Frame ("out of range length error") bit is set.
RxHalted	Reception Halted	R/W. Reception interrupted by clearing RxEn or setting RxHalt.
RxMCast	Multi-cast Received	R/W. Set if packet received is a Multi-cast Packet.
RxBCast	Broadcast Received	R/W. Set if packet received is a Broadcast Packet.

RxVLAN	VLAN Received	R/W. Set if packet received is a VLAN tagged Packet.
RxPAUSE	PAUSE Received	R/W. Set if packet received is a MAC Control PAUSE packet.
ARCStatus	ARC Status	R/W. Summary of ARC activity, (see encoding, below).
ARCEnt	ARC Entry	R/W. Index of ARC entry where address matched, all 1's if no match.
RxIPErr	Receive IP Error	R/W. Received an IP packet with an IP Checksum error.
RxTUErr	Receive TCP/UDP Error	R/W. Received an IP packet with a TCP or UDP payload with checksum error.

Reset to value 0000_0000h by hardware or software reset.

Cleared at beginning of each packet received.

The frame lengths above do not include preamble and Start Frame Delimiter (SFD).

The receive status flags are set whenever the corresponding event occurs. Once set, a flag stays set until another packet arrives. In addition, an interrupt is generated if the corresponding enable bit in the receive control register is set.

CtlRecd is set if the packet type is 8808h, and the ARC recognizes the address. If RxMCast and RxBCast (bits 17:18) are both zero, a Unicast Packet was received.

ARC Activity Status is encoded as follows:

- ❑ 0000 - toss, MAC Control received and PassCtl=0.
- ❑ 0001 - toss, length is less than “minLen”, but at least 6 bytes, and was keep otherwise.
- ❑ 0010 - toss, ARC match, Negative filtering.
- ❑ 0011 - reserved.
- ❑ 0100 - toss, External CAM hit, Negative filtering.
- ❑ 0101 - reserved.
- ❑ 0110 - toss, no match, no External CAM, no enable, positive filtering.
- ❑ 0111 - toss, packet length is too short for ARC result to be valid and shortEn is not set.
- ❑ 1000 - keep, Broadcast, Multicast, or Unicast enabled and matched.
- ❑ 1001 - reserved.
- ❑ 1010 - keep, ARC match, positive filtering.
- ❑ 1011 - reserved.
- ❑ 1100 - keep, External CAM hit, positive filtering.
- ❑ 1101 - reserved.
- ❑ 1110 - keep, no match, Negative filtering.
- ❑ 1111 - reserved.

Note: “minLen” is 64 bytes if ShortEn is not asserted, 14 bytes if ShortEn is asserted.

2.3.8 Station Management Data Access Register, “MD_Data”, 8058h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMI_Data[15:0]															

SMI_Data	Station Management Interface Data	R/W. Initialized to 0 by hardware reset. Initialized to 0 by software reset..
----------	-----------------------------------	---

Reset to value 0000_0000h by hardware or software reset.

The MII section of the IEEE 802.3 Standard for 100-BASE-T, 100-Mbit/s Ethernet, defines the format of the required station management data registers.

2.3.9 Station Management Control/Address Register, “MD_CA”, 805Ch

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
			PreSup	PhyBusy	RegWr	Phy_Addr[4:3]	
7	6	5	4	3	2	1	0
Phy_Addr[2:0]				Phy_Reg[4:0]			

Phy_Reg	PHY Register Address	R/W. Address of register inside the PHY to read or write.
Phy_Addr	PHY Device Address	R/W. Address of PHY device to read or write.
RegWr	Register Write	R/W. Writing a “1” indicated the MD_Data register is to be written to the PHY. Writing a “0” causes the PHY register to be read and the data placed in the MD_Data register.
PhyBusy	PHY Busy	R/W/SC. reset. Writing a “1” initiates the PHY register transfer. The hardware will clear the bit when the operation completes.
PreSup	Preamble Suppress	R/W. Writing a “1” suppresses the generation of the 32 bit PHY station management preamble before the PHY register transfer. The internal PHY of the 8430 does not require the preamble.

Hardware reset to value 0000_0000h.

Not affected by software reset.

Before attempting to access the PHY control registers, software should read the MD_CA register to ensure the busy bit is not set. The controller provides support for reading and writing of Station Management data to the PHY. Setting of options in station management registers does not affect the controller. Some PHYs may not support the option to suppress preambles after the first operation. The 78Q8430 PHY supports 1 bit of preamble.

2.3.10 ARC Address Register, “ARC_Adr”, 8060h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
On_Mem			ARC_Adr[10:6]				
7	6	5	4	3	2	1	0
ARC_Adr[5:0]							

ARC_Adr	ARC Memory Address	R/W. Address of four-byte location in ARC / OnNow memory to read or write.
On_Mem	OnNow Memory Select	R/W. When writing a “1” indicates the OnNow pattern memory is being addressed. Writing a “0” indicates the Address Recognition Circuit memory is being addressed.

Reset to value 0000_0000h by hardware or software reset.

The “ARC” and “On Now” parameters are stored in the DMA static ram. These parameters have indirect access from the programmers’ view, by using the ARC_Adr and ARC_Data registers.

In normal operating mode, the ARC_Data register is used to read or write the ARC contents, including the two double word locations for the Flow Control, that are immediately after the ARC data area. Writing to other memory locations in normal operating mode is inhibited.

When the “On_Mem” bit is set the address for the DMA static ram is offset to the first location of the “On Now” parameters, to allow relative addressing of the parameters. The range of the relative address is limited to “ARC_Adr[4:0]” in this mode.

When the “TestMode” bit of the DMA Control register is set, the ARC_Adr can be used to read or write the entire DMA static ram.

2.3.11 ARC Data Register, “ARC_Data”, 8064h

Byte 3	Byte 2	Byte 1	Byte 0
ARC_Data[0]	ARC_Data[1]	ARC_Data[2]	ARC_Data[3]
HNR_Data[0]	HNR_Data[1]	HNR_Data[2]	HNR_Data[3]
OnNow_Data[3]	OnNow_Data[2]	OnNow_Data[1]	OnNow_Data[0]

Reset to value 0000_0000h by hardware or software reset.

The ARC_DATA register is used to write and read Address Recognition Circuit data, Host Not Responding data, and OnNow data. The ARC data register has a copy of the data stored at the control memory bytes addressed by the ARC address register. The register may be read more than once, i.e. there is no auto-increment of addresses. When data is written to this register, the addressed control memory bytes are also changed.

2.3.12 ARC Enable Register, “ARC_Ena”, 8068h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
												ARC_En[20:16]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARC_En[15:0]															

ARC_En	ARC Enable bits	R/W. When written with a “1” the corresponding ARC memory location will be used for address filtering.
--------	-----------------	--

Hardware reset to value 0000_0000h.

Software reset has no effect.

The ARC enable register indicates which entries are valid for address filtering. Up to 21 entries, numbered 0 through 20, may be active.

2.3.13 PROM Control Register, "PROM_Ctl", 806Ch

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
PromBusy	Prom_Op[1:0]						
7	6	5	4	3	2	1	0
		Prom_Addr[5:0]					

Prom_Addr	Prom Address	R/W. Allows addressing of up to 64 16-bit entries.
Prom_Op	Prom Operation Code	R/W. 1 1 = Erase. 1 0 = Read. 0 1 = Write. 0 0 = Enable or Disable Writing, as specified in Prom_Addr: [5:4] = 11, Enable [5:4] = 00, Disable
PromBusy	Prom Busy bit	R/W/SC. Writing a "1" initiates the Prom data transfer. The hardware will clear the bit when the operation completes.

Hardware reset to value 0000_0000h.

Software reset has no effect.

The PROM control register provides control and status information and buffering for the PROM controller, which controls the reading and writing of an optional external EEPROM or small serial ROM device.

2.3.14 PROM Data Register, “PROM_Data”, 8070h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PROMDAT[15:0]															

PROMDAT	Prom Data	R/W. reset to value 0000_0000h by both hardware and software reset.
---------	-----------	---

Reset to value 0000_0000h by hardware or software reset.

The PROM Data registers provides the 16 bits of data written to or read from PROM. The current implementation supports the following devices: MicroChip 93LC46B and National NM93C46. Software drivers are responsible for reading the station address, storing it in the ARC, and enabling ARC operation, as part of the driver initialization.

2.3.15 Missed Error Count Register, “Miss_Cnt”, 8074h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MISSCNT[15:0]															

MISSCNT	Missed Error Count	R/W. Initialized to 0 by hardware reset. Not affected by software reset. This register counts the number of valid packets which are rejected by the MAC unit because of the noted error conditions. This count excludes packets the ARC rejects. The counter individual bytes are cleared by the action of reading the counter byte.
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The missed error count register provides a count of packets discarded due to various types of errors. Together with status information for packets transmitted and received. The missed error counter rolling over from 0x7FFF to 0x8000 sets the Missed Roll bit in the MAC control register. It also generates an interrupt if the Enable Missed Roll bit is set. If station management software requires more frequent interrupts, the missed error count register can be set to a value closer to the roll over value of 0x7FFF (ex: setting the register to 0x7F00 would provide for an interrupt after counting 256 occurrences). Reading the missed error count register clears the register. It is then the responsibility of software to maintain a global count with more bits of precision.

2.4 Network Statistics Control and Status Registers

2.4.1 Count Data Register, "CntData", 8080h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cnt_Data[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cnt_Data[15:0]															

Cnt_Data	Count Data	R/W. Contains the count value to be read or written per the Count Access Register control bits. Refer to the DMA Control Register for usage of the RmTxInit, RmRxInit, RMSwRq and RmenBank control bits.
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Reset to value 0000_0000h by hardware or software reset.

Contains the value of a Count Register read by a Read or Read and Clear operation. Contains the value to be written before a Write operation.

2.4.2 Count Access Register, “CntAcc”, 8084h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
					AutoInc	RdClr	CntWr
7	6	5	4	3	2	1	0
Cnt_Addr[7:0]							

Cnt_Addr	Memory Address of Counter	R/W. Address ranges: 00 to 1F, Transmit Counters. 20 to 3F, Receive Counters.
CntWr	Counter Write	R/W. When written with a “1” the counter is written. When written with a “0” the counter is read.
RdClr	Clear on Read	R/W. When written with a “1” the counter is cleared after being read. When written with a “0” the counter is not changed.
AutoInc	Auto Increment	R/W. When written with a “1” the address fields will be incremented after the operation. When written with a “0” the address field is not changed

Reset to value 0000_0000h by hardware or software reset.

The CntAcc register contains the address, opcode and control bits for read, read with clear, and write operations to the RMON memory area. Either Bank 0 or Bank 1 is addressed, as indicated by the RMemBank bit of the DMA_Ctl register.

2.4.3 Transmit RMON Interrupt Enable Register, “TxRmIntEn”, 8088h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TxRmIntEn[29:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxRmIntEn[15:0]															

TxRmIntEn	Transmit RMON Interrupt Enable	R/W. Each bit enables the generation of an interrupt when it's corresponding Interrupt Status bit is set.
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Hardware reset to value 0000_0000h.

Software reset has no effect.

2.4.4 Receive RMON Interrupt Enable Register, “RxRmIntEn”, 808Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RxRmIntEn[23:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxRmIntEn[15:0]															

RxRmIntEn	Receive RMON Interrupt Enable	R/W. Each bit enables the generation of an interrupt when it's corresponding Interrupt Status bit is set.
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Hardware reset to value 0000_0000h.

Software reset has no effect.

2.5 IP Checksum Control Registers

2.5.1 IP Checksum Control Register, "IPChkCtl", 8090h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
TxIPGenEn	TxIPChkEn	RxIPChkEn					
7	6	5	4	3	2	1	0
				IPTypeOff[3:0]			

IPTypeOff	IP Type Offset	R/W. Offset into the IP Type field (default = 0).
RxIPChkEn	Receive IP Check Enable	R/W. When written with a "1" will check IP and TCP/UDP checksums during reception.
TxIPChkEn	Transmit IP Check Enable	R/W. When written with a "1" will check IP and TCP/UDP checksums during transmission.
TxIPGenEn	Transmit IP Generate Enable	R/W. When written with a "1" will generate IP and TCP/UDP checksums during transmission.

Hardware reset to value 0000_0000h.

Software reset has no effect.

The IPTypeOff value is used by the transmit and receive circuits to locate the two byte field to check for IP Datagram type value (0800h). The IPTypeOff value is the number of bytes after the 12 byte field containing destination and source address. The default value of 0 corresponds to Ethernet encapsulation (RFC 894). Software can set this value to other values, such as 8 for IEEE 802.2/IEEE 802.3 encapsulation (RFC 1042).

The presence of a VLAN tag value (8100h) after the 12 byte field containing destination and source address, will cause the transmit and receive circuits to add 4 to the offset value. Other protocol stack variations must be accounted for by the Software, in setting the IPTypeOff value.

The TxIPChkEn bit has no effect if the TxIPGenEn bit is set.

2.6 Network Wake Up Registers

2.6.1 Wake Up Control Register, “WU_Ctl”, 80A0h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
				HostNR		Eevnt3	Eevnt2
15	14	13	12	11	10	9	8
Eevnt1		MPIdx					
7	6	5	4	3	2	1	0
		On_Ctl[4:0]					MPCtl

MPCtl	Magic Packet Control	R/W. When written with a “1”, enables Magic Packet_ wake up during EMI low power modes which support wake up features.
On_Ctl	OnNow Control	R/W. When written with a “1”, enables the corresponding OnNow pattern and results in the OnNow Pattern memory.
MPIdx	Magic Packet Index	R/W. ARC index value to use for Magic Packet compares.
LinkChgCtl	Link Change Control	R/W. When set to 1, enables the Link Status Change signal to generate a Wake Up event.
Eevnt[n]	External Event Control	R/W. When a bit is set to 1, it enables the corresponding External Event signal to cause a Power Management Event when the signal is asserted.
HostNR	Host Not Responding Control	R/W. When set to 1, enables the Tx circuit to transmit a Host Not Responding packet, when system does not respond to an INTB signal within the number of system clock cycles specified by HNR Cnt register.

Hardware reset to value 0000_0000h.

Software reset has no effect.

This register controls the activation of different Network Wake Up features, when EMI Power Management Low power states are enabled.

2.6.2 Wake Up Status Register, “WU_Stat”, 80A4h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
				HNRstat		Eevntst3	Eevntst2
15	14	13	12	11	10	9	8
Eevntst1	LinkChgd						
7	6	5	4	3	2	1	0
				ONStat			MPStat

MPStat	Magic Packet Status	Set when a Magic Packet_ wake up packet is recognized and MPCtl is set in the WU_Ctl register.
ONStat	OnNow Status	Set when the corresponding OnNow pattern, and the OnNow Results registers match the incoming packet, and the corresponding ONCtl bit is set.
LinkChgd	Link Changed	Set when the Link Status Change signal is asserted, and the LinkChgCtl bit is set.
Eevntst[3:1]	External Event Status	Set when an External Event signal is asserted, and the EECtl bit is set.
HNRStat	Host Not Responding Status	Set to 1 if INTB is not disabled within the number of clock cycles indicated by the HNRCnt register.

Hardware reset to value 0000_0000h.

Software reset has no effect.

This register can be examined by Software to determine the cause of the PMEB signal being asserted.

2.6.3 OnNow Result Registers [0:4], “On_Res[0:4]”, 80A8h, ACh, B0h, B4h, B8h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cnt_Data[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cnt_Data[15:0]															

The value is held in the internal parameter / staging RAM, so hardware and software resets have no effect.

Each register holds a 32-bit CRC value, which is the resulting CRC when an OnNow Packet is sent, with the corresponding OnNow mask pattern, and the desired packet data bytes.

2.6.4 Host Not Responding Initial Count Register, “On_Res[0:2]”, 80BCh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Cnt_Data[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cnt_Data[15:0]															

The value is held in the internal parameter / staging RAM, so hardware and software resets have no effect.

This 32-bit register holds the initial value for the Host Not Responding counter. The default value is ffff-ffff. The default provides about a 40 second delay with a system clock of 100 MHz, 80 second delay with a system clock of 50 MHz.

2.7 EMI Control and Status Registers

2.7.1 EMI Register Overview

Table 22 shows the register name, symbol, address, size, and access type for each EMI configuration register. They provide device identification, control and status information, and various setup registers, which are addressed at initialization time.

Table 22 : EMI Register Group

NAME	SYMBOL	ADDR	BYTES	ACCESS
EMI Identification	EMI_Id	8100h	4	RO
EMI Control		810Ch	4	R/W *
Power Management Capabilities		8140h	4	RO
Power Management Control and Status		8144h	4	R/W*

*indicates special semantics

The EMI Configuration Register addresses and the DMA, MAC, Flow Control, RMON, and PHY Register addresses are effective when the CSB and ADDRHI signals are asserted. Individual registers are selected by matching the low order address bits.

2.7.2 EMI Identification Register, “EMI_ID”, address 8100h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Prod_id[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ver_id[7:0]								Rev_id[7:0]							

Prod_id[15:0]	Product Identifier	R/O = 8430h. Indicates the product number.
Ver_id[7:0]	Version Identifier	R/O = 00h. Indicates the product version number.
Rev_id[7:0]	Revision Identifier	R/O = 01h. Indicates the silicon revision number.

The value is hardware coded, so hardware and software resets have no effect.

The Identification register consists of 3 read/only fields. The value of the product identifier field is the 16 bit hexadecimal value of the first 4 digits of the Teridian Semiconductor product number. The value of the version identifier is a number that corresponds to the modifier letter in the Teridian Semiconductor product number (00 = A of 8430A, 01 = B of 8430B, etc). The value of the revision identifier field is the revision of the devices's silicon mask set (01 = the first version).

2.7.3 EMI Control Register, “EMI_CS”, 810Ch

31	30	29	28	27	26	25	24
Bist_av	Bist_strt			Bist_err3	Bist_err2	Bist_err1	Bist_err0
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	7	6	5	4

Bist_av	BIST Available	R/O = 1 This bit indicates that this device contains built in self test circuitry for the embedded memory.
Bist_strt	BIST Start	R/W Write 1 to start BIST testing, the bit then indicates “test in progress” status, and the bit self-clears at the end of the BIST test.
Bist_err3	BIST test error detected	R/W BIST Error found in system ram.
Bist_err3	BIST test error detected	R/W BIST Error found in parameter / staging ram.
Bist_err3	BIST test error detected	R/W BIST Error found in RMON ram bank 1.
Bist_err3	BIST test error detected	R/W BIST Error found in RMON ram bank 0.

Hardware reset to value 0000_0000h.

Software reset has no effect.

The “Built In Self Test” (BIST) is used to test the on-chip memories. BIST should be invoked by the software driver before start-up initialization of the memories, as invoking BIST overwrites the RAM data and interferes with normal memory operation. When the “Bist_strt” bit self-clears, the status of the individual BIST controllers are latched into “Bist_err”. Any bit set indicates the associated BIST controller detected a memory test error.

2.7.4 EMI Power Management Capabilities Register, “PM_CAP”, 8140h

31	30	29	28	27	26	25	24
Pme_sup4	Pme_sup3	Pme_sup2	Pme_sup1	Pme_sup0	D2_supp	D1_supp	
23	22	21	20	19	18	17	16
		Ds_init		Pme_clk	Pm_ver2	Pm_ver1	Pm_ver0
15	14	13	12		10	9	8
Nxt_ptr[7:0]							
7	6	5	4	7	6	5	4
Cap_id[7:0]							

Pme_supp[4:0]	Power management event support	R/O = 00010b Indicates device only asserts PMEB from D1.
D2_supp	State D2 support	R/O = 0b Indicates device doesn't support D2 power state.
D1_supp	State D1 support	R/O = 1b Indicates device does support D1 power state.
Ds_init	Device specific initialization	R/O = 0b Indicates device has no specific initialization.
Pme_clk	Power management clock	R/O = 1b Indicates device relies on power management clock (BUSCLK) for PMEB operation.
Pm_ver[2:0]	Power management version	R/O = 010b Indicates PM Interface Spec. 1.1 compliance.
Nxt_ptr[7:0]	Next pointer	R/O = 48h Points to next capability
Cap_id[7:0]	Capability id	R/O = 01h Indicates power management capability.

2.7.5 EMI Power Management Control / Status Register, “PM_CSR”, 8144h

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
Psmarg[5:4]		Psmarg[3:2]		Psmarg[1:0]			
15	14	13	12		10	9	8
Pme_stat							Pme_enb
7	6	5	4	7	6	5	4
						Pm_ps1	Pm_ps0

Pme_stat	Power management event status	R/W1clr. Writing a “1” clears the bit. Writing a “0” has no effect. The bit is set when “wake-up” logic would normally set PMEB, regardless of the state of PMEB.
Psmarg[5:4]	Power Supply Margin	R/W. Writing a “11” margins the digital logic power supply high. Writing a “00” margins the power supply low.
Psmarg[3:2]	Power Supply Margin	R/W. Writing a “11” margins the parameter and RMON ram’s power supply high. Writing a “00” margins the power supply low.
Psmarg[1:0]	Power Supply Margin	R/W. Writing a “11” margins the host buffer ram power supply high. Writing a “00” margins the power supply low.
Pme_enb	Power management enable	R/W. Writing a “1” enables the assertion of PMEB when a “wake-up” condition is detected.
Pm_ps[1:0]	Power management present state	R/W. Sets the power management logic to one of the 4 supported states. 01b = D1, 00b = D0

Hardware reset to value 00A8_0000h.

Software reset has no effect.

2.8 PHY Management Registers

2.8.1 PHY Register Overview

The 78Q8430 PHY implements sixteen-bit registers which are accessible via the MAC Station Management Access Registers. The supported registers are shown below. Unsupported registers will be read as all zeroes. The 78Q8430 PHY responds to PHYAD value 00001.

The types of PHY Register access are summarized in Table 23:

Table 23 : PHY Register Group

Address	Symbol	Name	Default (Hex)
0	MR0	Control	(3100)
1	MR1	Status	(7849)
2	MR2	PHY Identifier 1	000E
3	MR3	PHY Identifier 2	7233
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0001
6	MR6	Auto-Negotiation Expansion	0000
7		(Not Implemented)	0000
8-15		(Reserved)	0000
16	MR16	Vendor Specific	(03C0)
17	MR17	Interrupt Control/Status Register	0000
18	MR18	Diagnostic Register	0000
19	MR19	PHY Transmit Trim Register	<4400>
20	MR20	(Reserved)	<0000>
21	MR21	(Reserved)	0000
22	MR22	(Reserved)	0000
23	MR23	PHY LED Configuration Register	0010
24	MR24	MDI/MDIX Control Register	

2.8.2 PHY Control Register, “MR0”, phy address 00h

MR0: Control Register

Bit	Symbol	Type	Default	Description
0.15	RESET	R/WC	0	Reset: Setting this bit to ‘1’ resets the device and sets all registers to the default states. This bit is self-clearing.
0.14	LOOPBK	R/W	0	Loopback: When this bit is set to ‘1’, no transmission of data on the network medium occurs and any receive data on the network medium is ignored. By default, the loopback signal path will encompass as much of the 78Q8430 PHY circuitry as possible. The loopback signal path may be changed through the Vendor Specific Register (MR16). This bit allows for a diagnostic test.
0.13	SPEEDSL	R/W	1	Speed Selection: This bit determines the speed of operation of the 78Q8430 PHY. Setting this bit to ‘1’ indicates 100Base-TX operation and a ‘0’ indicates 10Base-T mode. This bit will default to a ‘1’ upon reset. If auto-negotiation is enabled, this bit will be set by the PHY to reflect the result of auto-negotiation. If auto-negotiation is not enabled, this bit may be written to force manual configuration.
0.12	ANEGEN	R/W	1	Auto-negotiation enable: The auto-negotiation process is enabled when this bit is ‘1’. This bit is set upon reset. If this bit is cleared to ‘0’, manual speed and duplex mode selection is accomplished through bits 0.13 (<i>SPEEDSL</i>) and 0.8 (<i>DUPLEX</i>) of the Control Register
0.11	PWRDN	R/W	0	Power-down: The device may be placed in a low power consumption state by setting this bit to ‘1’. While in power-down state, the device will still respond to management transactions.
0.10	ISO	R/W	(0)	Isolate: When set to ‘1’, the device will present a high-impedance on its MII output pins. This allows for multiple PHY’s to be attached to the same MII interface. When the device is isolated, it still responds to management transactions. The default value of this bit is 0.
0.9	RANEG	R/WC	0	Restart Auto-negotiation: Normally, the Auto-Negotiation process is started at power up. Setting this bit to ‘1’ can restart the process. This bit is self-clearing.
0.8	DUPLEX	R/W	1	Duplex mode: This bit determines whether the device supports full- duplex or half-duplex. A ‘1’ indicates full-duplex operation and a ‘0’ indicates half-duplex. This bit will default to ‘1’ upon reset. If auto-negotiation is enabled, this bit will be set to reflect the result of auto-negotiation. If auto-negotiation is not enabled, this bit can be written to force manual configuration.

0.7	COLT	R/W	0	Collision Test: When this bit is set to '1', the device will assert the COL signal in response to the assertion of the TX_EN signal. Collision test is disabled if the PCSBP bit, MR23.9 is high. Collision test can be activated regardless of the duplex mode of operation.
0.6:0	RSVD	R	0	Reserved

2.8.3 PHY Status Register, "MR1", phy address 01h

MR1: Status Register

Bits 1.15 through 1.11 reflect the ability of the 78Q8430 PHY. They do not reflect any ability changes made via the MII Management interface to bits 0.13 (*SPEEDSL*), 0.12 (*ANEGEN*) and 0.8 (*DUPLEX*).

Bit	Symbol	Type	Default	Description
1.15	100T4	R	0	100BASE-T4 ability: Reads '0' to indicate the 78Q8430 PHY does not support 100BASE-T4 mode.
1.14	100X_F	R	1	100BASE-TX Full Duplex ability: 0 : Not able 1 : Able (default)
1.13	100X_H	R	1	100BASE-TX Half Duplex ability: 0 : Not able 1 : Able (default)
1.12	10T_F	R	1	10BASE-T Full Duplex ability: 0 : Not able 1 : Able (default)
1.11	10T_H	R	1	10BASE-T Half Duplex ability: 0 : Not able 1 : Able (default)
1.10	100T2_F	R	0	100BASE-T2 Full Duplex ability: Reads '0' to indicate the 78Q8430 PHY does not support 100BASE-T2 full duplex mode.
1.9	100T2_H	R	0	100BASE-T2 Half Duplex ability: Reads '0' to indicate the 78Q8430 PHY does not support 100BASE-T2 half duplex mode.
1.8	EXTS	R	0	Extended Status Information availability: Reads '0' to indicate the 78Q8430 PHY does not support Extended Status information in MR15.

1.7	RSVD	R	0	Reserved
1.6	MFPS	R	1	Management Frame Preamble Suppression support: Reads '1' to indicate the 78Q8430 PHY can read management frames without preambles. The management interface needs a minimum of 32 bits of preamble after reset.
1.5	ANEGC	R	0	Auto-negotiation Complete: Logic one indicates that the Auto-Negotiation process has been completed, and that the contents of registers MR4,5,6 are valid.
1.4	RFAULT	RC/LH	0	Remote Fault: A logic one indicates that a remote fault condition has been detected and when so, it remains set until it is cleared. This bit can only be cleared by reading this register (MR1).
1.3	ANEGA	R	(1)	Auto-negotiation Ability: When set, this bit indicates the device's ability to perform Auto-Negotiation. The value of this bit is determined by the <i>ANEGEN</i> bit (MR0.12).
1.2	LINK	RC/LL	0	Link Status: A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remains cleared until it is read.
1.1	JAB	RC/LH	0	Jabber Detect: In 10Base-T mode, this bit is set during a jabber event. After a jabber event, the bit remains set until cleared by a read operation.
1.0	EXTD	R	1	Extended capability: Reads '1' to indicate the 78Q8430 PHY provides an extended register set (MR2 and beyond).

2.8.4 PHY Identifier Registers, "MR2,3", phy address 02h,03h

MR2: PHY Identifier Register 1

Bit	Symbol	Type	Value	Description
2.15:0	OUI [23:6]	R	000Eh	Organizationally Unique Identifier: This value is 00-C0-39 for Teridian Semiconductor Corporation. This register contains 16 of the upper 18 bits of the identifier.

MR3: PHY Identifier Register 2

Bit	Symbol	Type	Value	Description
3.15:10	OUI [5:0]	R	1Ch	Organizationally Unique Identifier: The remaining 6 bits of the 24-bit OUI.
3.9:4	MN	R	23h	Model Number: The "23" from the model number are encoded into the 6 bits.
3.3:0	RN	R	3h	Revision Number: The value '0011' corresponds to the third revision of the silicon.

2.8.5 PHY Auto-Negotiation Advertisement Registers “MR4”, phy address 04h

MR4: PHY Auto-Negotiation Advertisement Register

Bit	Symbol	Type	Default	Description
4.15	NP	R	0	Next Page: Not supported. Reads logic zero.
4.14	RSVD	R	0	Reserved.
4.13	RF	R/W	0	Remote Fault: Setting this bit to ‘1’ allows the device to indicate to the link partner a Remote Fault Condition.
4.12:5	TAF	R/W	(0Fh)	Technology Ability Field: The default value of this field is dependent upon the MR1.15:11 register bits. This field can be overwritten by management to auto-negotiate to an alternate common technology. Writing to this register has no effect until auto-negotiation is re-initiated.
4.12	A7	R	0	Reserved for future technology.
4.11	ASYMP	R/W	0	Asymmetric PAUSE operation for full duplex Links. Default is 0=not supported. If the MAC supports Asymmetric PAUSE, this bit can be written as 1. Writing to this register has no effect until auto-negotiation is re-initiated.
4.10	PAUSE	R/W	0	PAUSE Operation for Full Duplex links. Default is 0= not supported. If the MAC supports PAUSE, this bit can be written as 1. Writing to this register has no effect until auto-negotiation is re-initiated.
4.9	A4	R	0	100BASE-T4: The 78Q8430 PHY does not support 100BASE-T4 operations.
4.8	A3	R/W	1	100BASE-TX Full Duplex: This bit will be set to ‘1’ upon reset and will be writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
4.7	A2	R/W	1	100BASE-TX Half Duplex: This bit will be set to ‘1’ upon reset and will be writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
4.6	A1	R/W	1	10BASE-T Full Duplex: This bit will be set to ‘1’ upon reset and will be writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
4.5	A0	R/W	1	10BASE-T: This bit will be set to ‘1’ upon reset and will be writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
4.4:0	S4:0	R	01h	Protocol Selector Field: The value is ‘00001’ for IEEE 802.3.

2.8.6 PHY Auto-Negotiation Line Partner Ability Register “MR5”, phy address 05h

5.15	NP	R	0	Next Page: When ‘1’ is read, it indicates the link partner wishes to engage in Next Page exchange.
5.14	ACK	R	0	Acknowledge: When ‘1’ is read, it indicates the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
5.13	RF	R	0	Remote Fault: When ‘1’ is read, it indicates the link partner has a fault.
5.12:5	A7:0	R	0	Technology Ability Field: This field contains the technology ability of the link partner. The bit definition is the same as MR4.12:5.
5.4:0	S4:0	R	00h	Selector Field: This field contains the type of message sent by the link partner. For IEEE 802.3 compliant link partner, this field should be ‘00001’.

When MR5 contains a next page message, the bit definition is the same as MR7.

2.8.7 PHY Auto-Negotiation Expansion Register “MR6”, phy address 06h

Bit	Symbol	Type	Default	Description
6.15:5	RSVD	R	0	Reserved
6.4	PDF	RC/LH	0	Parallel Detection Fault: When ‘1’ is read, it indicates that more than one technology has been detected during link up. This bit is cleared when read.
6.3	LPNPA	R	0	Link Partner Next Page Able: When ‘1’ is read, it indicates the link partner supports the Next Page function.
6.2	NPA	R	0	Next Page Able: Reads ‘0’ since the 78Q8430 PHY does not support Next Page function.
6.1	PRX	RC/LH	0	Page Received: Reads ‘1’ when a new link code word has been received into the Auto-negotiation Link Partner Ability Register. This bit is cleared upon read.
6.0	LPANEGA	R	0	Link Partner Auto-negotiation Able: When ‘1’ is read, it indicates the link partner is able to participate in the Auto-Negotiation function.

2.8.8 PHY Vendor Specific Register “MR16”, phy address 10h

Bit	Symbol	Type	Default	Description
16.15	RPTR	R/W	0	Repeater Mode: When set, the 78Q8430 PHY is put into Repeater mode of operation. In this mode, full duplex is prohibited, CRS responds to receive activity only and, in 10Base-T mode, the SQE test function is disabled.
16.14	INPOL	R/W	0	When this bit is '0', the internal PHY interrupt signal is forced low to signal an interrupt. Setting this bit to '1' causes the PHY interrupt signal to be forced high to signal an interrupt. The PHY interrupt status signal is mapped to the PhyIntEn bit in the Int_En register.
16.13	RSVD	R	0	Reserved.
16.12	TXHIM	R/W	0	Transmitter High-Impedance Mode: When set, the TXOP/TXON transmit pins and the TX_CLK pin are put into a high-impedance state. The receive circuitry remains fully functional.
16.11	SQEI	R/W	0	SQE Test Inhibit: Setting this bit to '1' disables 10Base-T SQE testing. By default, this bit is '0' and generating a COL pulse following the completion of a packet transmission performs the SQE test.

2.8.9 PHY Interrupt Control / Status Register “MR17”, phy address 11h

The Interrupt Control/Status Register provides the means for controlling and observing the events, which trigger an interrupt on the internal PHY interrupt signal. This register can also be used in a polling mode via the MII Serial Interface as a means to observe key events within the PHY via one register address. Bits 0 through 7 are status bits, which are each set to logic one based upon an event. These bits are cleared after the register is read. Bits 8 through 15 of this register, when set to logic one, enable their corresponding bit in the lower byte to signal an interrupt on the PHY interrupt signal. The level of this interrupt can be set via the MR16.14 (*INPOL*) bit.

Bit	Symbol	Type	Def ault	Description
17.15	JABBER_IE	R/W	0	Jabber Interrupt Enable
17.14	RXER_IE	R/W	0	Receive Error Interrupt Enable
17.13	PRX_IE	R/W	0	Page Received Interrupt Enable
17.12	PDF_IE	R/W	0	Parallel Detect Fault Interrupt Enable
17.11	LP_ACK_IE	R/W	0	Link Partner Acknowledge Interrupt Enable
17.10	LS_CHANGE_IE	R/W	0	Link Status Change Interrupt Enable
17.9	RFAULT_IE	R/W	0	Remote Fault Interrupt Enable
17.8	ANEG-COMP_IE	R/W	0	Auto-Negotiation Complete Interrupt Enable
17.7	JAB_INT	RC	0	Jabber Interrupt: This bit is set high when a Jabber event is detected by the 10Base-T circuitry.
17.6	RXER_INT	RC	0	Receive Error Interrupt: This bit is set high when the RX_ER signal transitions high.
17.5	PRX_INT	RC	0	Page Received Interrupt: This bit is set high when a new page has been received from the link partner during auto-negotiation.
17.4	PDF_INT	RC	0	Parallel Detect Fault Interrupt: This bit is set high by the auto-negotiation logic when a parallel detect fault condition is indicated.
17.3	LP_ACK_INT	RC	0	Link Partner Acknowledge Interrupt: This bit is set high by the auto-negotiation logic when FLP bursts are received with the acknowledge bit set.
17.2	LS_CHANGE_INT	RC	0	Link Status Change Interrupt: This bit is set when the link status transitions from an OK status to a FAIL status, or vice versa.
17.1	RFAULT_INT	RC	0	Remote Fault Interrupt: This bit is set when a remote fault condition is detected.
17.0	ANEG_COMP_INT	RC	0	Auto-Negotiation Complete Interrupt: This bit is set by the auto-negotiation logic upon - completion of auto-negotiation.

2.8.10 PHY Diagnostic Register “MR18”, phy address 12h

This register contains both user accessible and non-user accessible bits (Reserved) for internal testmode activation. The user-accessible bits are located at bit 15-8 locations.

Bit	Symbol	Type	Default	Description
18.15:13	RSVD	R	0	Reserved
18.12	ANEGF	RC	0	Auto-Negotiation Fail Indication: This bit is set when auto-negotiation completes and no common technology was found. It remains set until read.
18.11	DPLX	R	0	Duplex Indication: This bit indicates the result of the auto-negotiation for duplex arbitration as follows: 0 : half-duplex was the highest common denominator 1 : full-duplex was the highest common denominator
18.10	RATE	R	0	Rate Indication: This bit indicates the result of the auto-negotiation for data rate arbitration as follows: 0 : 10Base-T was the highest common denominator 1 : 100Base-TX was the highest common denominator
18.9	RXSD	R	0	Receiver Signal Detect Indication: In 10Base-T mode, this bit indicates that Manchester data has been detected. In 100Base-TX mode, it indicates that the receive signal activity has been detected (but not necessarily locked on to).
18.8	RXLCK	R	0	Receive PLL Lock Indication: Indicates that the Receive PLL has locked onto the receive signal for the selected speed of operation (10Base-T or 100Base-TX).
18.7:0	RSVD	R	0	Reserved

2.8.11 PHY Transmit Trim Register “MR19”, phy address 13h

Bit	Symbol	Type	Default	Description
19.15:14	TXO[1:0]	R/W	01	Transmit Amplitude Selection: Sets the transmit output amplitude to account for transmit transformer insertion loss. 00 : Gain set for 0.0dB of insertion loss 01 : Gain set for 0.4dB of insertion loss 10 : Gain set for 0.8dB of insertion loss 11 : Gain set for 1.2dB of insertion loss
19.13:0	RSVD	R/W	XXX	Reserved

2.8.12 PHY LED Configuration Register “MR23”, phy address 17h

Bit	Symbol	Type	Default	Description
23.15:8	RSVD	R/W	0	Reserved
23.7:4	LED1[3:0]	R	<1h>	0000 = Link OK 0001 = RX or TX Activity (Default LED1) 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = 100 BASE-TX mode 0110 = 10 BASE-T mode 0111 = Full Duplex 1000 = Link OK/Blink=RX or TX Activity
23.3:0	LED0[3:0]	R	<0h>	0000 = Link OK (Default LED0) 0001 = RX or TX Activity 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = 100 BASE-TX mode 0110 = 10 BASE-T mode 0111 = Full Duplex 1000 = Link OK/Blink=RX or TX Activity

2.8.13 PHY MDI / MDIX Control Register “MR24”, phy address 18h

Bit	Symbol	Type	Default	Description
24.15:9		R	0	Unused
24.8	SU_ATIMER	R/W	0	Write a ‘1’ to this bit to speed up A_sync timer by 1.28 seconds. Only writeable if test mode is enabled by MR23.15.
24.7	PD_MODE	R/W	1	Write a ‘1’ to this bit to add Parallel Detect mode. This will allow auto-switching to work when auto-negotiation is off while the other device has it on.
24.6	AUTO_SW	R/W	1	Write a ‘1’ to this bit to enable auto switching.
24.5	MDIX	R/W	0	Indicates state of the MDI pair or force configuration: 1= MDIX (cross over) 0= MDI When auto_sw is a ‘1’, this bit will only be readable. When auto_sw is a ‘0’ this bit can be written to set the configuration.
24.4	MDIX_CM	R	0	Indicates completion of auto-switch sequence. 1 = Sequence completed 0 = Sequence in progress or auto-switch is disabled.
24.3:0	MDIX_SD	R/W	<0000>	Write initial pattern seed for switching algorithm. Initial seed will directly effect attempts [9,8,5,4] respectively to written bits [3:0]. Setting to [0000] will result in device using its own seed of [0101].

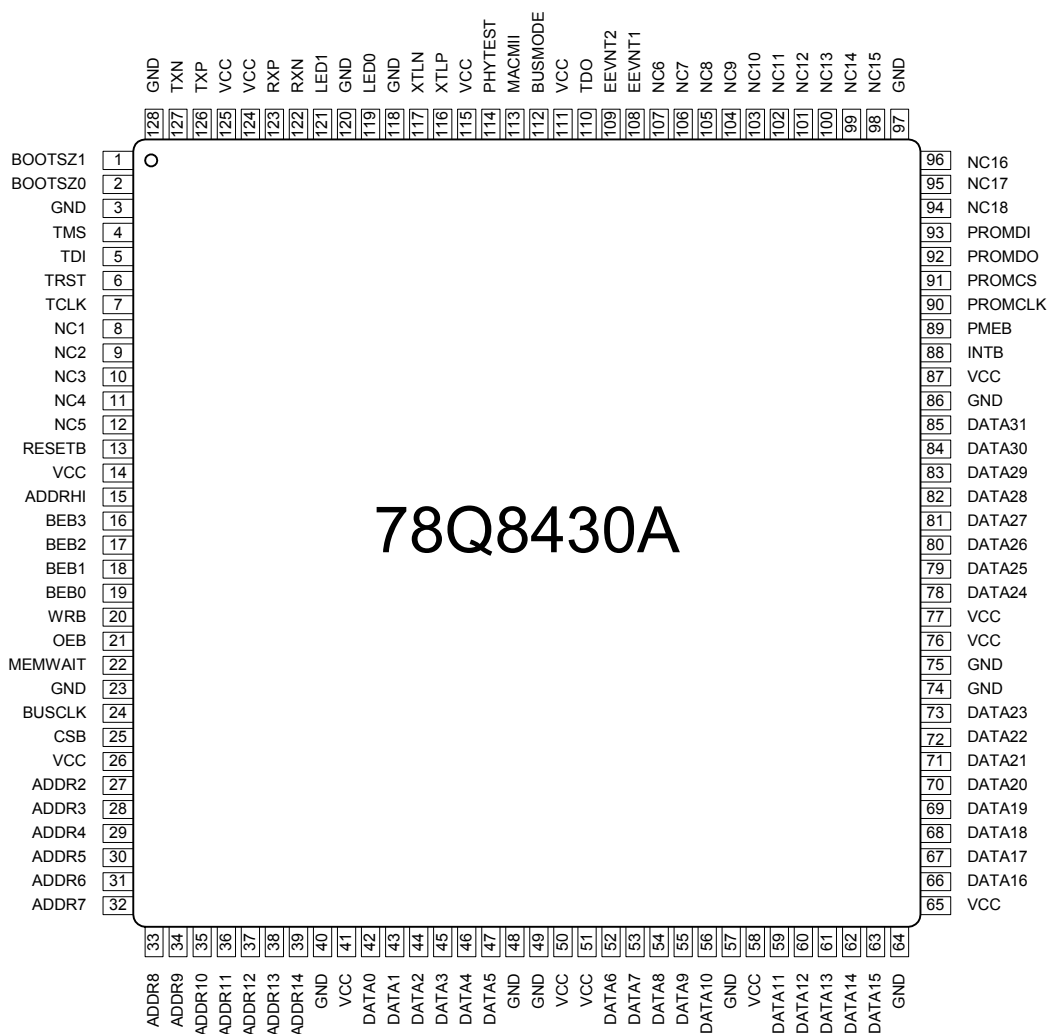
2.8.14 PHY BER BIST Control Register “MR25”, phy address 19h

Bit	Symbol	Type	Default	Description
25.15:14		R	0	Unused
25.13	BIST_EN	R/W	0	Write a '1' to this bit to enable BER BIST mode. This will enable both BER transmit data and receive error counting. Only writeable if test mode is enabled by MR23.15.
25.12	TXEN_INT	R/W	0	Controls source of transmit enable for BER BIST mode. Write a '1' to this bit to have the PHY transmit maximum sized packets. (1518 bytes with .96 us gap). Only writeable if test mode is enabled by MR23.15.
25.11:0	ER_CNT	R	0	Reports number of errors counted in BER BIST mode. The part must be connected to another PHY with the same feature transmitting. Part will count up to 4095 errors and stop. Reset PHY to return to zero.

3 PACKAGE DESCRIPTION

3.1 128 Pin LQFP (JEDEC LQFP) Package Pin Designations

Figure 17 : 128 Pin Diagram



4 PIN DESCRIPTION

4.1 Pin Legend

Table 24 : Pin Legend

Type	Description	Type	Description
A	Analog	I	TTL-level Input
IU	TTL-level Input, with Pull-up	ID	TTL-level Input, with Pull-down
IS	TTL-level Input, with Schmitt Trigger	B	TTL-level Bidirectional Pin
O	TTL-level Output	OZ	TTL-level Output (Tristate)
OD	TTL-level Output (Open Drain)		
S	Supply	G	Ground

The pin descriptions are for the standard / default embedded PHY mode of operation (subsequently referred to as: “**mission mode**”). Some pins have alternate functionality while in mission mode, and are described in this section. Alternate modes of operation of the pins in “**non-mission mode**” are discussed in later sections. Alternate modes of operation are configured either by device pin connections, configuration register programming, or link partner auto-negotiation state. Naming of pins in a group that with a numeric index are done in a “little endian” fashion.

4.2 Clock Pins

Table 25 : Clock Pin Descriptions

Signal	Pin	Type	Description
XTLP	116	A	Crystal Positive/Negative : Standard connections to an external 25 MHz crystal. Alternative connection to an external 25 MHz TTL clock source. The 78Q8430 senses the state of the XLTN pin. If it is connected to ground, the 78Q8430 will automatically disable the internal oscillator, and configure itself to use the XLTP pin as an external clock input. Provides timing reference for all media dependant interface operations.
XTLN	117		
BUSCLK	24	I	Peripheral Clock : Provides timing reference for all 78Q8430 host bus operations when in host bus synchronous mode, or host bus asynchronous mode and external clocking selected. The other host pins are referenced to this clock pin when the host interface is in the synchronous mode.

4.3 Media Dependent Interface (MDI) Pins

Table 26 : MDI Pin Descriptions

Signal	Pin	Type	Description
TXP	126	A	Transmit Output Positive/Negative : Transmitter outputs for both 10BASE-T and 100BASE-TX. MDI-X Mode: Receive Input Positive/Negative: Receiver inputs for both 10BASE-T and 100BASE-TX.
TXN	127	A	
RXP	123	A	Receive Input Positive/Negative : Receiver inputs for both 10BASE-T and 100BASE-TX. MDI-X Mode: Transmit Output Positive/Negative : Transmitter outputs for both 10BASE-T and 100BASE-TX.
RXN	122	A	

4.4 LED Display (PHY) Pins

Table 27 : LED Pin Descriptions

Signal	Pin	Type	Description
LED0	119	OZ	PHY display LED0 (Link OK) : The default for LED0 is Link OK (led is on for link established).
LED1	121	OZ	PHY display LED1 (Link OK) : The default for LED1 is activity (led is on when there is either RX or TX activity).

The LED pins use standard logic drivers. They output a logic low when the LED is meant to be on and are tristate when it is meant to be off. The LED cathode should be connected to the output pin, and a series resistor from the power supply connected to the LED anode.

4.5 EMI Data Pins

Table 28 : EMI Data Pin Descriptions

Signal	Pin	Type	Description
DATA31	85	B	Data Bus DATA[31:0] : External Memory Interface: CPU data during the bus data phase.
DATA30	84		
DATA29	83		
DATA28	82		
DATA27	81		
DATA26	80		
DATA25	79		
DATA24	78		
DATA23	73		
DATA22	72		
DATA21	71		
DATA20	70		
DATA19	69		
DATA18	68		
DATA17	67		
DATA16	66		
DATA15	63		
DATA14	62		
DATA13	61		
DATA12	60		
DATA11	59		
DATA10	56		
DATA9	55		
DATA8	54		
DATA7	53		
DATA6	52		
DATA5	47		
DATA4	46		
DATA3	45		
DATA2	44		
DATA1	43		
DATA0	42		

4.6 EMI Address and Byte Enable Pins

Table 29 : EMI Address & Byte Enable Pins

Signal	Pin	Type	Description
ADDRHI	15	I	Address High : The 78Q8430 samples this line on the leading edge (falling edge) of CSB to obtain the address mode. When this line is 1, the address bus denotes a register address. When this line is 0, the address bus denotes an internal memory address. This bit should be connected to a higher order address line, to reflect the desired mapping of the device into the CPU's address space.
ADDR14	39	I	Address Bus : The 78Q8430 samples the address lines on the leading edge of CSB to obtain a specific register or memory address. ADDR14 is the MSB, and ADDR2 is the LSB, of a 13-bit address space (32 Kbytes). In 32-bit bus mode, ADDR[14:2] are the 32-bit double-word address, and the BEB[3:0] lines provide the byte lane selection. In 16-bit bus mode, BEB[3] is used as ADDR[1] to provide a 16-bit word address, and the BEB[1:0] lines provide the byte lane selection. In 8-bit bus mode, BEB[3:2] are used as ADDR[1:0] to provide an 8-bit byte address, and BEB[1:0] are unused.
ADDR13	38	I	
ADDR12	37	I	
ADDR11	36	I	
ADDR10	35	I	
ADDR9	34	I	
ADDR8	33	I	
ADDR7	32	I	
ADDR6	31	I	
ADDR5	30	I	
ADDR4	29	I	
ADDR3	28	I	
ADDR2	27	I	
BEB3	16	B	Byte Enable 3 (active low) : In 32-bit bus mode, this is the lane selection for bits [31:24]. In 16-bit and 8-bit bus modes, this pin becomes ADDR[1].
BEB2	17	I	Byte Enable 2 (active low) : In 32-bit bus mode, this is the lane selection for bits [23:16]. In 16-bit bus mode, this pin is unused. In 8-bit bus mode, this pin becomes ADDR[0].
BEB1	18	B	Byte Enable 1 (active low) : In 32-bit and 16-bit bus modes, this is the lane selection for bits [15:8]. In 8-bit bus mode, this pin is unused.
BEB0	19	I	Byte Enable 0 (active low) : In 32-bit and 16-bit bus modes, this is the lane selection for bits [7:0]. In 8-bit bus mode, this pin is unused.

4.7 EMI Control Pins

Table 30 : EMI Control Pin Descriptions

Signal	Pin	Type	Description
RESETB	13	I	Reset (active low) : Referred to as hardware reset. Causes all 78Q8430 outputs to enter a high-impedance state, stops all current operations, and initializes registers.
CSB	25	I	Chip Select (active low) : The Processor asserts this signal to initiate a read or write operation. The assertion edge of CSB is used to latch the bus address, the byte enables, and the read/write select line.
WRB	20	I	Write Enable (active low) : The Processor asserts WRB to indicate a write operation. The negation (high) indicates a read operation.
OEB	21	I	Output Enable (active low) : The Processor asserts OEB to enable the 78Q8430 data drivers on a read operation.
MEMWAIT	22	O	Memory Wait : During a bus cycle the 78Q8430 asserts MEMWAIT to indicate that it is not ready to drive or receive valid data on the DATA lines. The polarity is dependant on the BUSMODE pin. When BUSMODE = '1' the pin is asserted high. When BUSMODE = 0 the pin is asserted low.
INTB	88	OD	Interrupt (active low) : The 78Q8430 asserts the INTB signal when it detects a interrupt event. External pull-up resistor required.
PMEB	89	OD	Power Management Event (active low) : The 78Q8430 asserts the PMEB signal when it detects a "wake-up" event. External pull-up resistor required.

4.8 Mode Pins

Table 31 : Chip Mode Pin Descriptions

Signal	Pin	Type	Description
BUSMODE	112	I	BUSMODE, PHY_TEST, MAC_MII chip configuration : 0,0,0 = IBM sync bus, int. phy, ext. system clock 0,0,1 = IBM sync bus, ext. phy, ext. system clock 0,1,0 = test mode : reserved 0,1,1 = test mode : reserved 1,0,0 = ST async bus, int. phy, ext. system clock 1,0,1 = ST async bus, ext. phy, ext. system clock 1,1,0 = ST async bus, int. phy, int. system clock 1,1,1 = ST async bus, ext. phy, int. system clock
PHY_TEST	114	I	
MAC_MII	113	I	
BOOTSZ1	1	B	BOOTSZ[1:0] : is strapped to indicate the EMI bus size: 00 - bus is 32 bits wide. 01 - bus is 16 bits wide. Only DATA[15:0] are used. 10 - bus is 8 bits wide. Only DATA[7:0] are used. 11 - (reserved).
BOOTSZ0	2	B	

4.9 EEPROM Pins

Table 32 : EEPROM Interface Pin Descriptions

Signal	Pin	Type	Description
PROM_CS	91	OZ	EEPROM Chip Select : Used to frame transmissions to and from an external EEPROM (93LC46B or equivalent).
PROM_CLK	90	OZ	EEPROM Clock : Clock for transmitting to and from an external EEPROM/ROM. This is compatible with the slowest commercial parts, which specify a maximum frequency of 1 MHz.
PROM_DI	93	B	EEPROM Data In : Data line for transmitting from the external EEPROM to the controller. Must be high with no EEPROM present. External pull-up resistor required.
PROM_DO	92	OZ	EEPROM Data Out : Transfers data from the controller to an external EEPROM/ROM.

4.10 JTAG Pins

Table 33 : JTAG Pin Descriptions

Signal	Pin	Type	Description
TRST	6	I	Test Reset : System provided reset for JTAG logic. External pull-down resistor required.
TCLK	7	I	Test Clock : System provided clock for JTAG logic. External pull-down resistor required.
TMS	4	IU	Test Mode Select : Enables JTAG boundary scan using serial in/serial out ports. Sampled on rising edge of TCLK.
TDI	5	IU	Test Data In : Serial input port for clocking in test data to be shifted to the output at the end of the boundary scan chain (TDO).
TDO	110	O	Test Data Out : Serial output port for clocking out test data shifted from the input at the beginning of the boundary scan chain (TDI).

4.11 Multifunction Pins

Table 34 : Multifunction Pin Descriptions

Signal	Pin	Type	Internal PHY mode : External PHY mode
NC1	8	I	No Connect : MII receive data valid.
NC2	9	I	No Connect : MII receive data bit 0.
NC3	10	I	No Connect : MII receive data bit 1.
NC4	11	I	No Connect : MII receive data bit 2.
NC5	12	I	No Connect : MII receive data bit 3.
NC6	107	O	No Connect : MII system management interface clock.
NC7	106	B	No Connect : MII system management interface data.
NC8	105	I	No Connect : MII receive carrier sense.
NC9	104	I	No Connect : MII collision detected.
NC10	103	O	No Connect : MII transmit data bit 3.
NC11	102	O	No Connect : MII transmit data bit 2.
NC12	101	O	No Connect : MII transmit enable.
NC13	100	I	No Connect : MII transmit clock.
NC14	99	O	No Connect : MII transmit error.
NC15	98	I	No Connect : MII receive error detected.
NC16	96	I	No Connect : MII receive clock.
NC17	95	OZ	No Connect : MII transmit data bit 1.
NC18	94	OZ	No Connect : MII transmit data bit 0.

Note: Inputs should be grounded if external PHY is not used, except for pin 106. Add pull-down resistor to pin 106 when external PHY is not used.

4.12 External Event Pins

Table 35 : External Event Pin Descriptions

Signal	Pin	Type	Description
EEVNT1	108	I	External Event #1 : When enabled, a change in state on EEVNT1 can cause the assertion of either INTB or PMEB. When an external PHY is connected, this pin expected to be used as the system management interrupt pin.
EEVNT2	109	I	External Event #2 : When enabled, a change in state on EEVNT1 can cause the assertion of either INTB or PMEB.

Note: Add external pull-down resistors to pins 108 and 109 if inputs are not used.

4.13 Power Pins

Table 36 : Power Pin Descriptions

Signal	Pin	Type	Description
VCC	125	S	+3.3V supply for analog transmit section.
GND	128	G	Ground return for analog transmit section.
VCC	124	S	+3.3V supply for analog receive section.
GND	120	G	Ground return for analog receive section.
VCC	115	S	+3.3V supply for analog transmit section.
GND	118	G	Ground return for analog receive section.
VCC	111	S	+3.3V supply for digital logic section 1.
GND	97	G	Ground return for digital logic section 1.
VCC	14 26 50 76	S	+3.3V supply for digital logic section 2.
GND	3 23 49 75	G	Ground return for digital logic section 2.
VCC	41 51 58 65 77 87	S	+3.3V supply for high load digital IO.
GND	40 48 57 64 74 86	G	Ground return for high load digital IO.

5 ELECTRICAL SPECIFICATION

5.1 Absolute Maximum Ratings

Operation above maximum rating may permanently damage the device.

Table 37 : Absolute Maximum Ratings

PARAMETER	RATING
DC Supply Voltage (Vcc)	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150°C
Pin Voltage (except TXOP/N and RXIP/N)	-0.3 to (Vcc+0.6) VDC
Pin Voltage (TXOP/N and RXIP/N only)	-0.3 to (Vcc+1.4) VDC
Pin Current	± 120 mA

5.2 Recommended Operation Conditions

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

Table 38 : Recommended Operating Conditions

PARAMETER	RATING
DC Voltage Supply (Vcc)	3.3 ± 0.3 VDC
Ambient Operating Temperature (Ta)	[0:70]°C

5.3 DC Characteristics

Table 39 : DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	I_{CC}	Vcc = 3.3V; Auto-Negotiation		90	tbd	mA
		10BT (Idle)		90	tbd	
		10BT (Normal Activity)		100	tbd	
		100BTX		135	tbd	
Supply Current	I_{CC}	Power-down mode			tbd	mA

5.4 Digital I/O Characteristics

Table 40 : Digital I/O Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0			V
Input Current	Iil, Iih		-1		1	μ A
Input Capacitance	Cin			8		pF

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 8mA			0.4	V
Output Voltage High	Voh	Ioh = -8mA	2.4			V
Output Transition Time	Tt	CL = 20pF			6	ns
Tristate Output Leakage Current	Iz	Type tristate only	-1		1	μ A

6 TIMING SPECIFICATION

6.1 EMI Clock Timing

Figure 18 : EMI Clock Timing

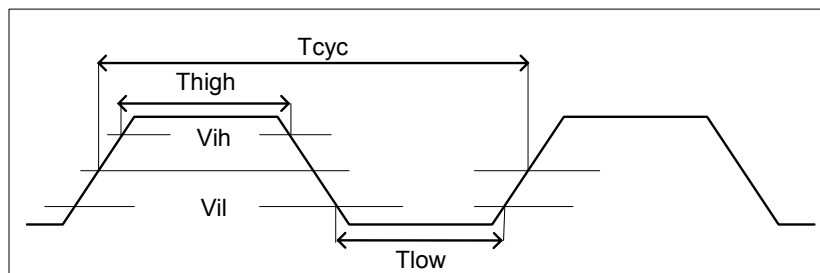


Table 41 : EMI Clock Timing

		SYNC 50		ASYNC 100		UNITS	
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
BUSCLK Cycle Time	T_{cyc}	20	-	10	-	ns	-
BUSCLK Frequency	-	-	50	-	100	MHz	-
BUSCLK High Time	T_{high}	8		3		ns	-
BUSCLK Low Time	T_{low}	8		3		ns	-
BUSCLK Slew Rate	-	1	3	1	3	V/ns	-

Table 42 : Reset Timing

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
RESETB Minimum Duration After BUSCLK is stable.	T_{reset}	1			BUSCLK clocks

6.2 EMI General Timing Parameters

Figure 19 : EMI Read Timing

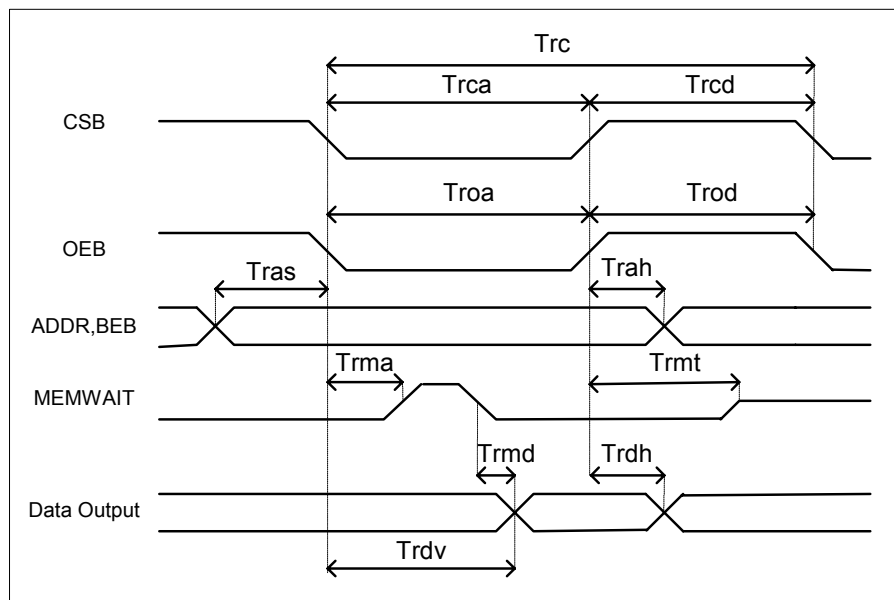


Table 43 : EMI Read Timing

PARAMETER	SYMBOL	SYNC 50		ASYNCR 100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	Trc	5		7		clocks	
CSB Assertion Time	Trca	2		4		clocks	
CSB Deassertion Time	Trcd	3		3		clocks	
OEB Assertion Time	Troa	1		2		clocks	
OEB Deassertion Time	Trod	1		2		clocks	
ADDR,BEB Setup to CSB,OEB Valid	Tras	1		1		clocks	
ADDR Hold Time	Trah	0		0			
CSB,OEB valid to Data Valid (MEMWAIT does not assert)	Trdv		15		15	ns	
CSB, OEB valid to MEMWAIT assert	Trma		13		13	ns	1
MEMWAIT deassert to Data valid	Trmd		0		0	ns	1
CSB deassert to MEMWAIT tristate	Trmt		8		8	ns	1
Data Output Hold	Trdh	0		0		ns	

Figure 20: EMI Write Timing

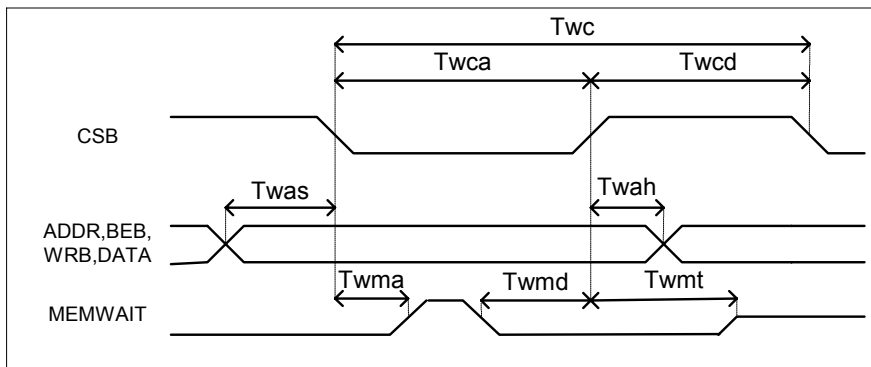


Table 44 : EMI Write Timing

		SYNC 50		ASYNCR 100			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Write Cycle Time	Twc	3		5		clocks	
CSB Assertion Time	Twca	2		4		clocks	
CSB Deassertion Time	Twcd	1		1		clocks	
ADDR,BEB,WRB,DATA Setup to CSB Valid	Twas	1		1		clocks	
ADDR,BEB,WRB,DATA Hold Time	Twah	0		0		ns	
CSB, WRB valid to MEMWAIT asserted (MEMWAIT may not assert)	Twma		13		13	ns	1
CSB deassert to MEMWAIT tristate	Twmt		8		8	ns	1
MEMWAIT deassert to CSB deassert	Twmd	0		0		ns	1

Note.

1. For both read and write cycles, MEMWAIT is asserted low (bus wait) when BUSMODE = 0 (Sync mode) and is asserted high (bus wait) when BUSMODE=1 (Async mode).

6.3 EMI Timing Measurement Conditions

Figure 21: EMI Output Timing

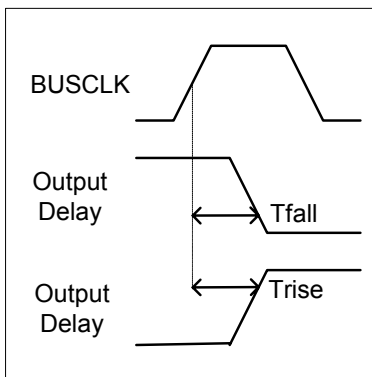


Figure 22: EMI Input Timing

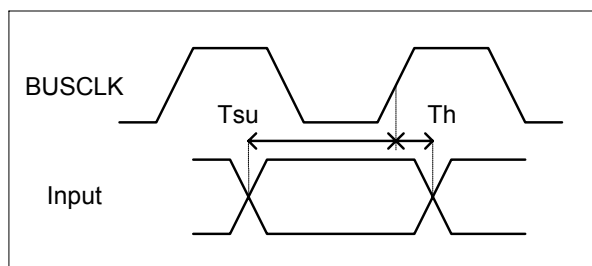


Table 45 : EMI General Timing

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 16mA			0.4	V
Output Voltage High	Voh	Ioh = -16mA	2.4			V
Output Rise Time	Trise	CL = 35pF			5.7	ns
Output Fall Time	Tfall	CL = 35pF			6.2	ns
Input Setup Time	Tsu		10			ns
Input Hold Time	Th		10			ns

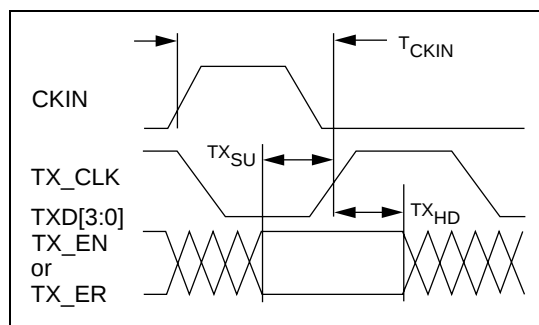
6.4 MII Digital Timing Characteristics

6.4.1 MII Transmit Interface

Table 46 : MMI Transmit Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX _{SU}		15			ns
Hold Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX _{HD}		0			ns
CKIN-to-TX_CLK Delay	T _{CKIN}		0		40	ns
TX_CLK Duty-Cycle			40		60	%

Figure 23: MMI Transmit Timing

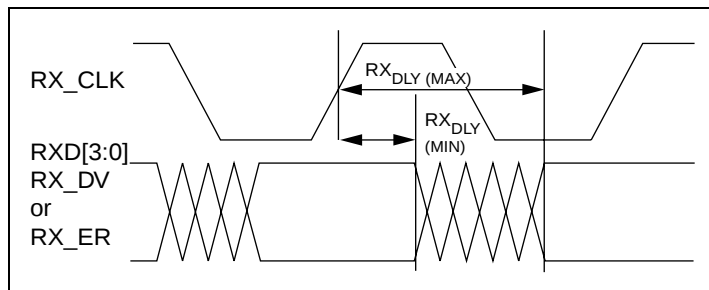


6.4.2 MII Receive Interface

Table 47 : MMI Receive Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Output Delay: RX_CLK to RXD[3:0], RX_DV, RX_ER	RX _{DLY}		10		30	ns
RX_CLK Duty-Cycle			40		60	%

Figure 24: MMI Receive Timing

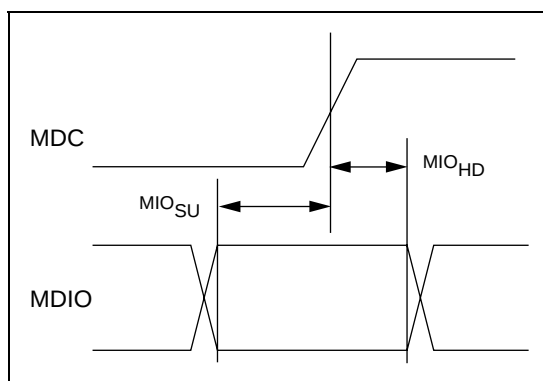


6.4.3 MII Management Input Interface

Table 48 : MMI MDIO Input Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: MDC to MDIO	MIO _{SU}		10			ns
Hold Time: MDC to MDIO	MIO _{HD}		0			ns
Max Frequency: MDC	F _{max}				25	MHz

Figure 25: MMI MDIO Input Timing

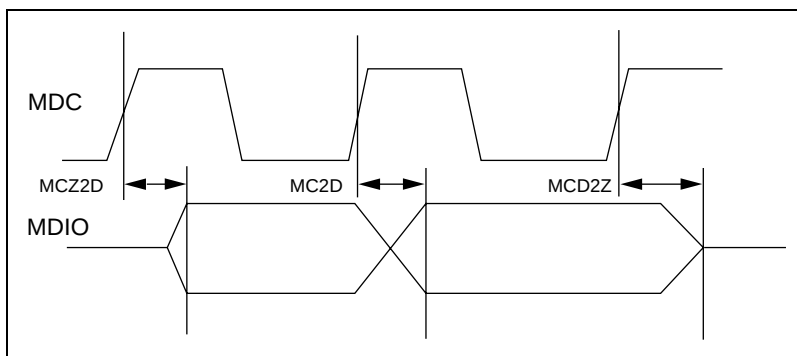


6.4.4 MII Management Output Interface

Table 49 : MMI MDIO Output Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
MDC to MDIO data delay	MC2D				30	ns
MDIO output from high Z to driven after MDC	MCZ2D				30	ns
MDIO output from driven to high Z after MDC	MCD2Z				30	ns

Figure 26: MMI MDIO Output Timing



6.4.5 MII 100Base-TX System Timing

Table 50 : MMI 100Base-TX System Timing

PARAMETER	CONDITION	NOM	UNIT
TX_EN Sampled to first bit of "J" on MDI output		12	BT
First bit of "J" on MDI input to CRS assert		15	BT
First bit of "T" on MDI input to CRS de-assert		23	BT
First bit of "J" on MDI input to COL assert		16	BT
First bit of "T" on MDI input to COL de-assert		24	BT
TX_EN Sampled to CRS assert	RPTR = low	4	BT
TX_EN sampled to CRS de-assert	RPTR = low	4	BT

Note : System timing requirements for 100BASE-TX operation are listed in Table 24-2 of Clause 24 of IEEE 802.3.

6.4.6 MII 10Base-T System Timing

Table 51 : MMI 10Base-T System Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TX_EN (MII) to TD Delay				6	BT
RD to RXD at (MII) Delay				6	BT
Collision delay				9	BT
SQE test wait			1		μs
SQE test duration			1		μs
Jabber on-time*		20		150	ms
Jabber off-time*		250		750	ms

Note : Guarantee by design. The specifications in the following table are included for information only.

6.5 Analog Electrical Characteristics

6.5.1 100Base-TX Transmitter

Table 52 : MMI 100Base-TX Transmit Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak Output Amplitude ($ V_{p+} $, $ V_{p-} $) (see note below)	Best-fit over 14 bit times; 0.4 dB Transformer loss	950		1050	mVpk
Output Amplitude Symmetry	$\frac{ V_{p+} }{ V_{p-} }$	0.98		1.02	
Output Overshoot	Percent of V_{p+} , V_{p-}			5	%
Rise/Fall time (t_r , t_f)	10-90% of V_{p+} , V_{p-}	3		5	ns
Rise/Fall time Imbalance	$ t_r - t_f $			500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence			± 250	ps
Jitter	Scrambled Idle			1.4	ns

Note : Measured at the line side of the transformer. Test Condition : Transformer P/N : TLA-6T103. Line Termination: $100\Omega \pm 1\%$

6.5.2 100Base-TX Transmitter (Informative)

Table 53 : MMI 100Base-TX Transmitter (Informative)

PARAMETER	CONDITION	MIN	MAX	UNIT
Return Loss	2 < f < 30 MHz	16		dB
	30 < f < 60 MHz	$16 - 20 \log\left(\frac{f}{30 \text{ MHz}}\right)$		
	60 < f < 80 MHz	10		
Open-Circuit Inductance	-8 < I _{in} < 8 mA	350		μH

Note : The specifications in the preceeding table is included for information only. They are mainly a function of the external transformer and termination resistors used for measurements

6.5.3 100Base-TX Receiver

Table 54 : MMI 100Base-TX Receiver Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Signal Detect Assertion Threshold		600	700	800	mVppd
Signal Detect De-assertion Threshold		300	350	400	mVppd
Differential Input Resistance			20		kΩ
Jitter Tolerance (pk-pk)		4			ns
Baseline Wander Tracking		-75		+75	%
Signal Detect Assertion Time	Not tested			1000	μs
Signal Detect De-assertion Time	Not tested			1.4	μs

6.5.4 10Base-T Transmitter

Table 55 : MMI 10Base-T Transmitter Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak Differential Output Signal (see note below)	All data patterns	2.2		2.8	V
Harmonic Content (dB below fundamental)	Any harmonic All ones data Not tested	27			dB
Link Pulse Width			100		ns
Start-of-Idle Pulse Width	Last bit 0		300		ns
	Last bit 1		350		ns

Note : The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3. Measured at the line side of the transformer. Test Condition : Transformer P/N : TLA-6T103. Line Termination: 100Ω±1%

6.5.5 10Base-T Transmitter (Informative)

Table 56 : MMI 10Base-T Transmitter (Informative)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output return loss		15			dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29 - 17 \log\left(\frac{f}{10}\right)$			dB
Peak Common-mode Output Voltage				50	mV
Common-mode rejection	15 V _{pk} , 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			100	mV
Common-mode rejection jitter	15 V _{pk} , 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			1	ns

Note : The specifications in the preceeding table is included for information only. They are mainly a function of the external transformer and termination resistors used for measurements

6.5.6 10Base-T Receiver

Table 57 : MMI 10Base-T Receive Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DLL Phase Acquisition Time			10		BT
Jitter Tolerance (pk-pk)		30			ns
Input Squelched Threshold		600	700	800	mVppd
Input Unsquelched Threshold		300	350	400	mVppd
Differential Input Resistance			20		k Ω
Bit Error Ratio			10 ⁻¹⁰		
Common-mode rejection	Square wave 0 < f < 500 kHz Not tested	25			V

6.6 Isolation Transformers

Table 58 : Isolation Transformers

NAME	VALUE	CONDITION
Turns Ratio	1 CT : 1 CT $\pm$ 5%	
Open-Circuit Inductance	350 μ H (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 μ H (max)	@ 1 MHz (min)
Inter-Winding Capacitance	12 pF (max)	
D.C. Resistance	0.9 Ω (max)	
Insertion Loss	0.5 dB (typ)	0 - 65 MHz
HIPOT	1500 Vrms	

Note : Two simple 1:1 isolation transformers are all that are required at the line interface, but transformers with integrated common-mode choke are recommended for exceeding FCC requirements. This table gives the recommended line transformer characteristics. The 100Base-TX amplitude specifications assume a transformer loss of 0.4 dB. For the transmit line transformer with higher insertion losses, up to 1.2 dB of insertion loss can be compensated by selecting the appropriate setting in the Transmit Amplitude Selection bits in register MR19.11:10

6.7 Reference Crystal

Table 59 : Reference Crystal

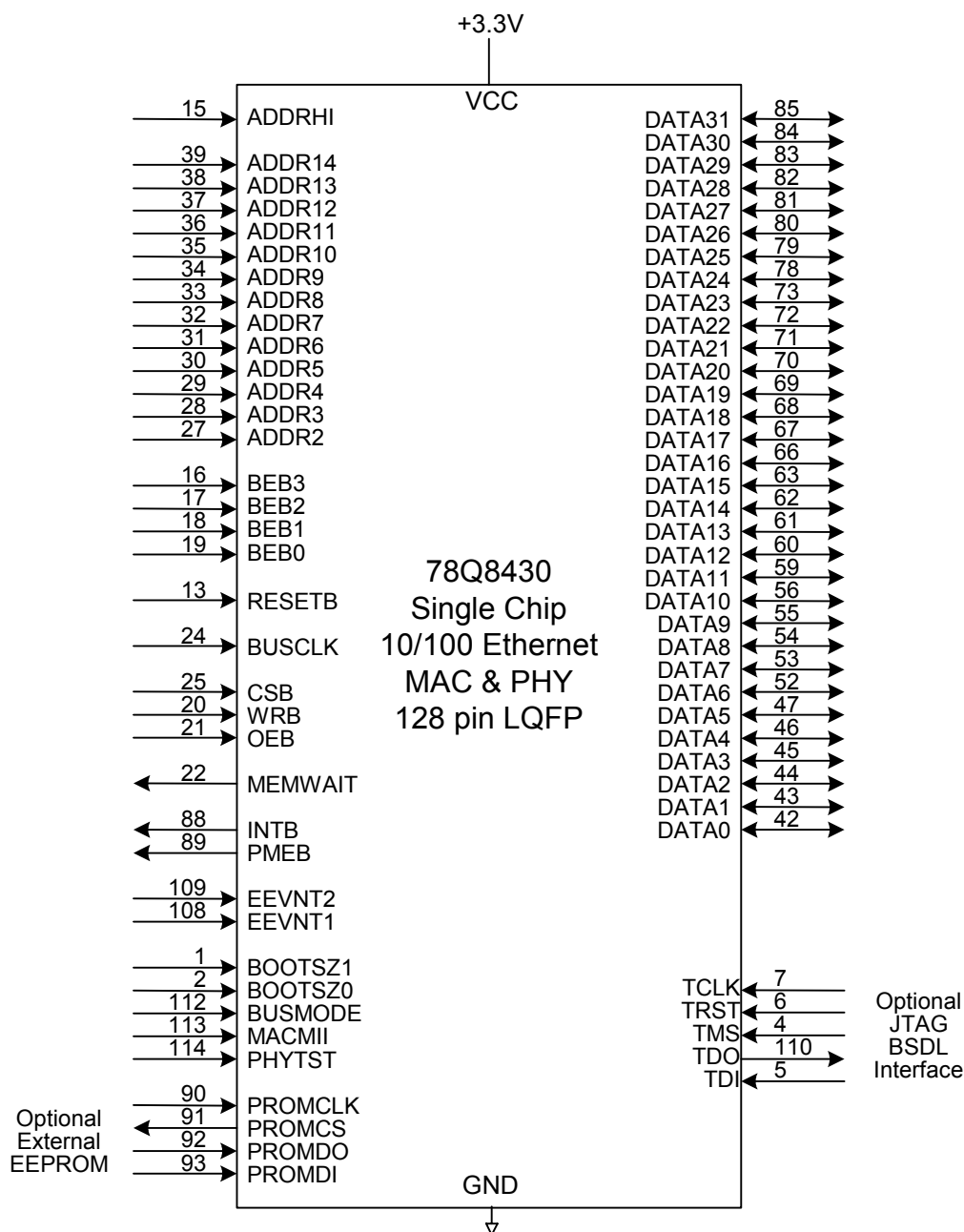
NAME	VALUE	UNITS
Frequency	25.00000	MHz
Load Capacitance*	4**	pF
Frequency Tolerance	±50	PPM
Aging	±2	PPM/yr
Temperature Stability (0 - 70°C)	±5	PPM
Oscillation Mode	Parallel Resonance, Fundamental Mode	
Parameters at 25°C ± 2°C ; Drive Level = 0.5 mW		
Shunt Capacitance (max)	10	pF
Motional Capacitance (min)	10	fF
Series Resistance (max)	60	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

Note: If the internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen.

* : Equivalent differential capacitance across the XTLP/XTLN pins

** : If crystal with a larger load is used, external shunt capacitors to ground should be added to make up the equivalent capacitance difference

7 SYSTEM BUS INTERFACE SCHEMATIC

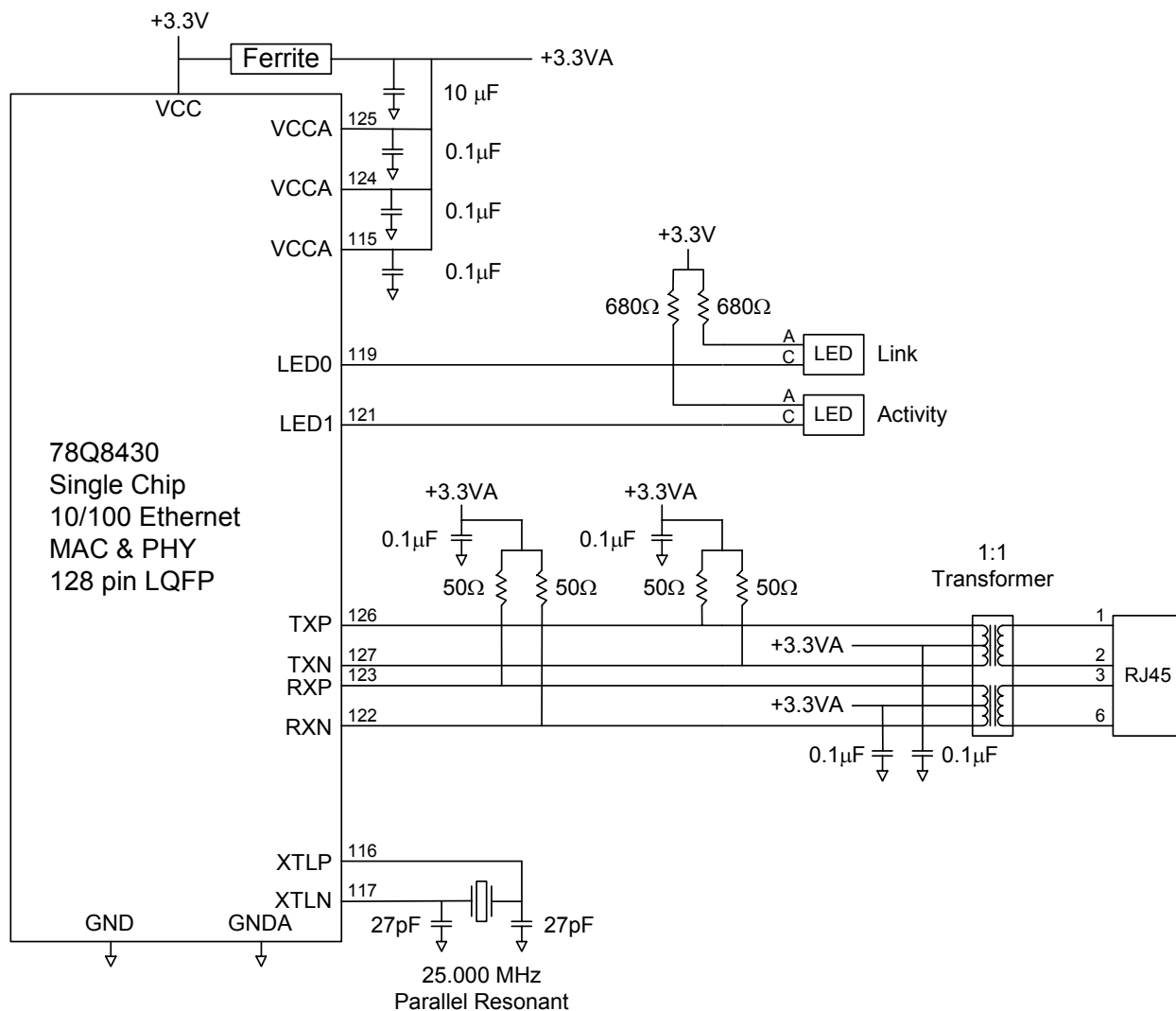


32 Bit Bus: BTSZ0=BTSZ1=GND
 16 Bit Bus: BTSZ0=VCC, BTSZ1=GND
 8 Bit Bus: BTSZ0=GND, BTSZ1=VCC

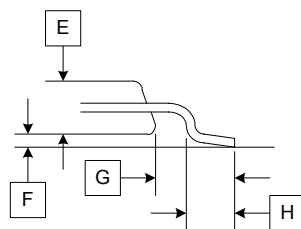
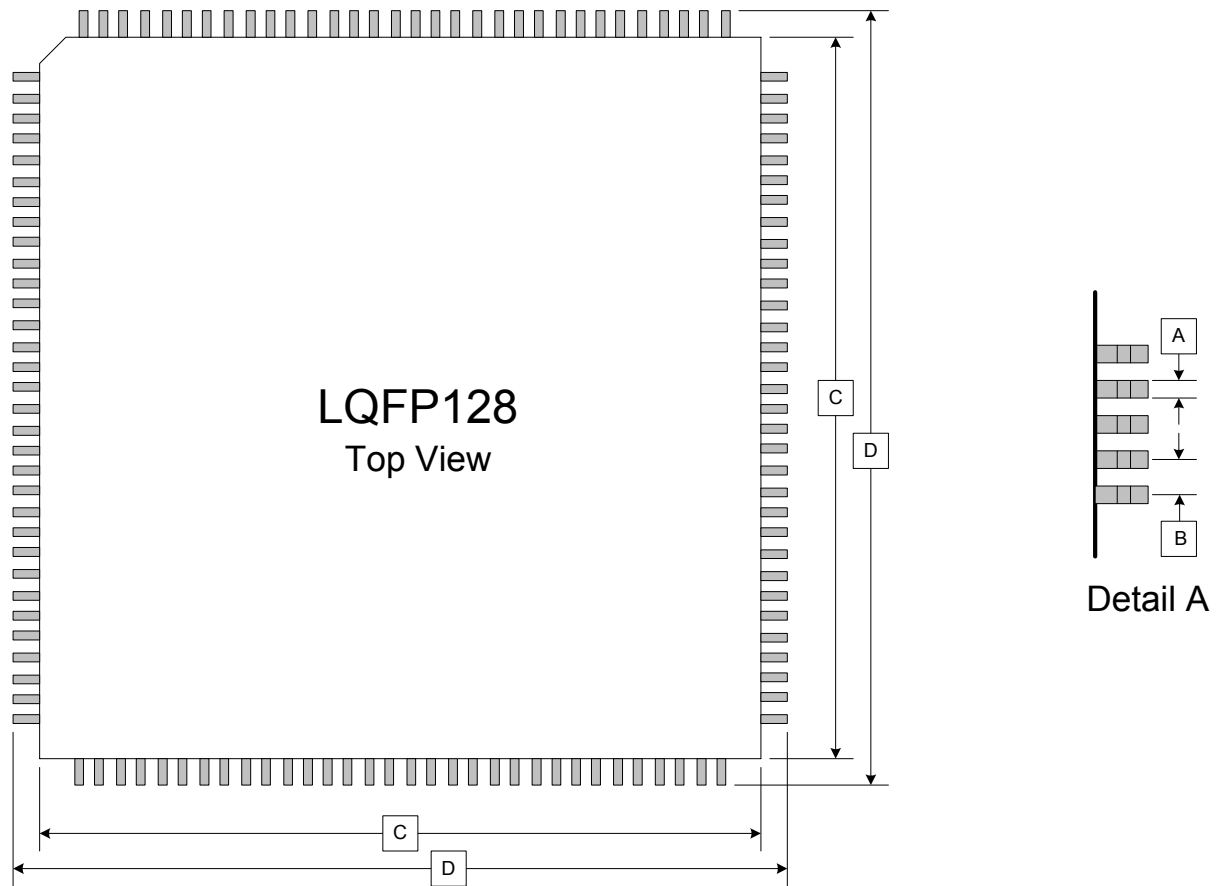
ST - Async, Little Endian: BUSMODE=VCC
 PPC - Sync, Big Endian: BUSMODE=GND

Ext BUSCLK: PHYTST=GND
 IntClkGen (Async Bus Only): PHYTST=VCC

8 LINE INTERFACE SCHEMATIC



9 PACKAGE MECHANICAL DRAWING – 128 PIN LQFP



Detail B

SYMBOL	MIN.	NOM.	MAX.
A	0.13	0.18	0.23
B		0.40 BSC.	
C		14.00 BSC.	
D		16.00 BSC.	
E	1.35	1.40	1.45
F	0.05		0.15
G		1.00	
H	0.45	0.60	0.75

ALL DIMENSIONS IN MILLIMETERS

10 ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
78Q8430, Revision 2, 128-LQFP, Commercial Temp	78Q8430-CGT	78Q8430-CGT xxxxxxxxxxx2
78Q8430, Lead-Free Revision 2, 128-LQFP, Commercial Temp	78Q8430-CGT/F	78Q8430-CGT xxxxxxxxxxx2F

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