

Introduction

The Teridian 78Q2123 and 78Q2133 MicroPHY can perform the following loopback operations for system diagnostic purposes:

- 1) MII interface 100Base-TX internal digital loopback
- 2) MII interface 10Base-T internal digital loopback
- 3) MII interface 10Base-T Natural Loopback (special case)
- 4) External loopback (using a cable loopback plug)

Remote loopback (remote PHY echos data) is a system operation and does not require any special configuration. The MicroPHY operates in its normal mode during remote loopback operations.

Loopback Data Path

The internal digital loopback path (TXD3:0 is looped back to RXD3:0) employed by the MicroPHY is shown in Figure 1. When loopback is enabled (by setting MII control register bit MR0.14 to "1") the analog interface circuitry is isolated from the data path. The TXOP/N outputs are disabled resulting in no link and no transmitted TXD3:0 data. Similarly, packet data present at RXIP/N is not forwarded to RXD3:0.

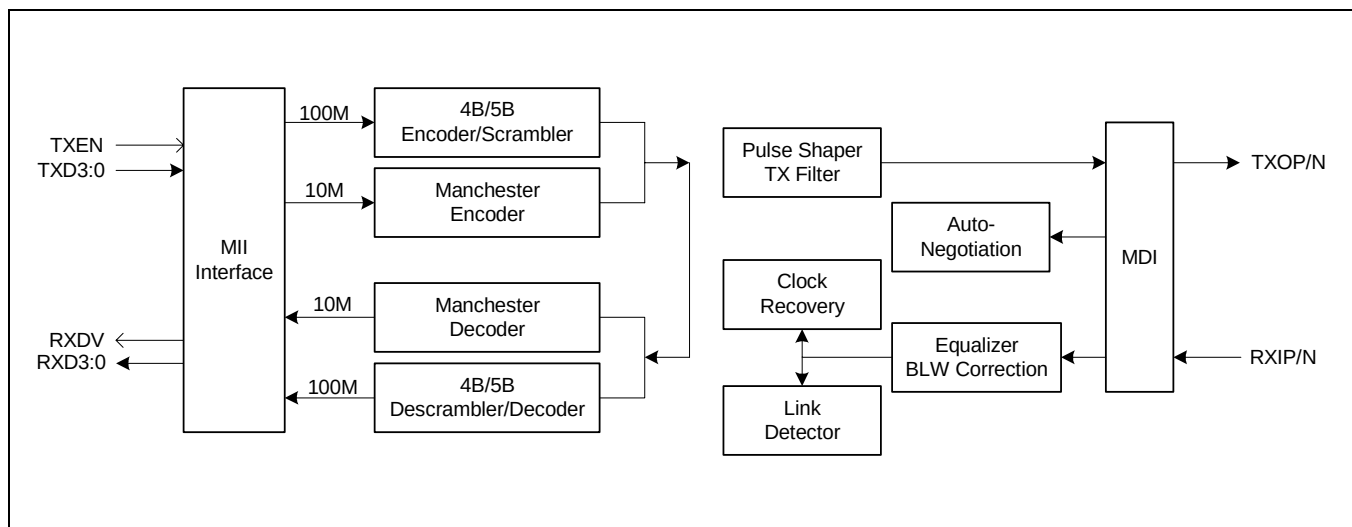


Figure 1 – MicroPHY Loopback Path

Loopback Modes

MII INTERFACE 100BASE-TX INTERNAL DIGITAL LOOPBACK

100Base-TX loopback is enabled when MR0.14 and MR0.13 are set to logic "1". Both full-duplex and half-duplex modes work for 100Base-TX loopback operation. Once bit MR0.14 is set, the Link LED is asserted and received packets are immediately available on the MII interface. When 100Base-TX loopback is enabled, the 2123's transmitter is disabled. Any connected PHY will drop link when loopback is enabled. Figure 2 shows the 100Base-TX internal 100Base-TX loopback path.

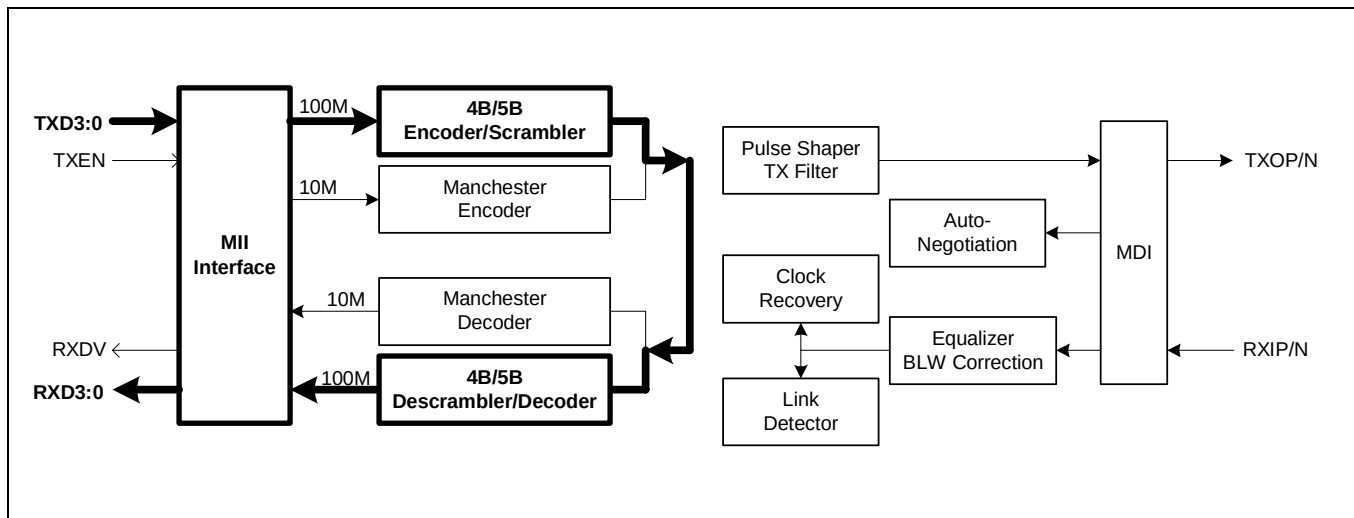


Figure 2 – MicroPHY 100Base-TX Loopback Path

MII INTERFACE 10BASE-TX INTERNAL DIGITAL LOOPBACK

10Base-T internal loopback is enabled when MR0.14 is set to logic “1” and MR0.13 is a logic “0”. Both full-duplex and half-duplex modes work for 10Base-T loopback operation. The Link LED is only asserted during packet reception.

The MicroPHY does not assert RXDV upon reception of the first packet. The NLP detector is excluded from the 10Base-T loopback path requiring reception of a packet to assert the “link up” status. Transmitting a “dummy” packet performs this link up assertion. Without “link up”, RXDV is disabled resulting in no reception of the first transmitted packet. Subsequent packets are received correctly while “link up” is valid. For two or more packets to be received, their inter-packet gap must be less than 65 msec to prevent the Drop Link Timer from expiring and to maintain “link up”.

When 10Base-T loopback is enabled, the 2123’s transmitter is disabled. Do not attach an external loopback plug while switching to 10Base-T internal loopback operation. Any connected PHY will drop link when loopback is enabled. Figure 3 shows the 10Base-T internal loopback path.

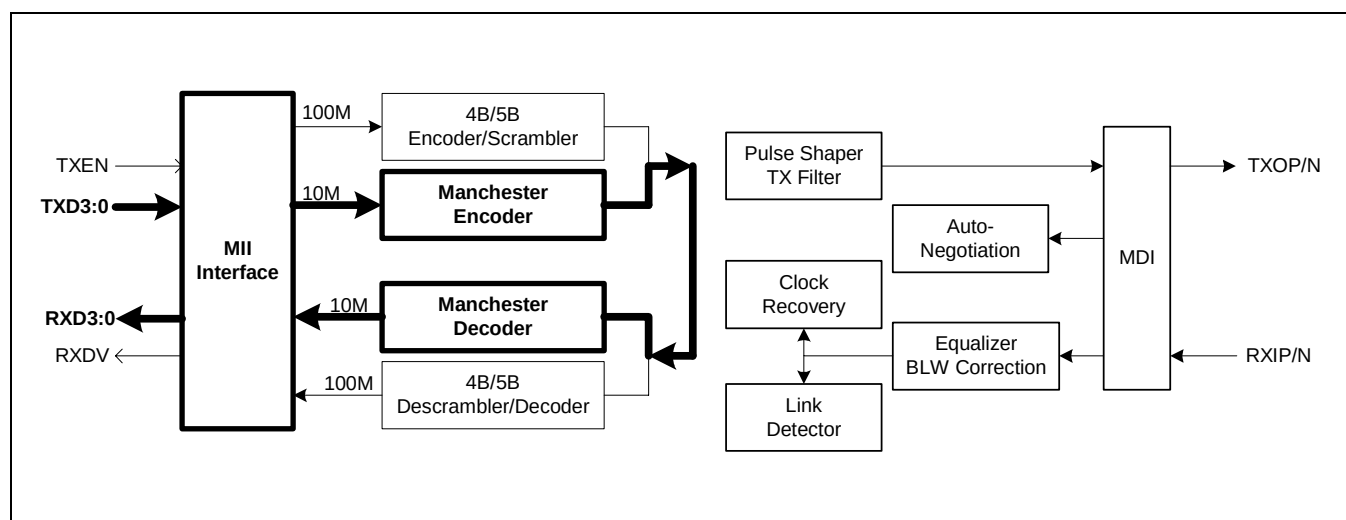
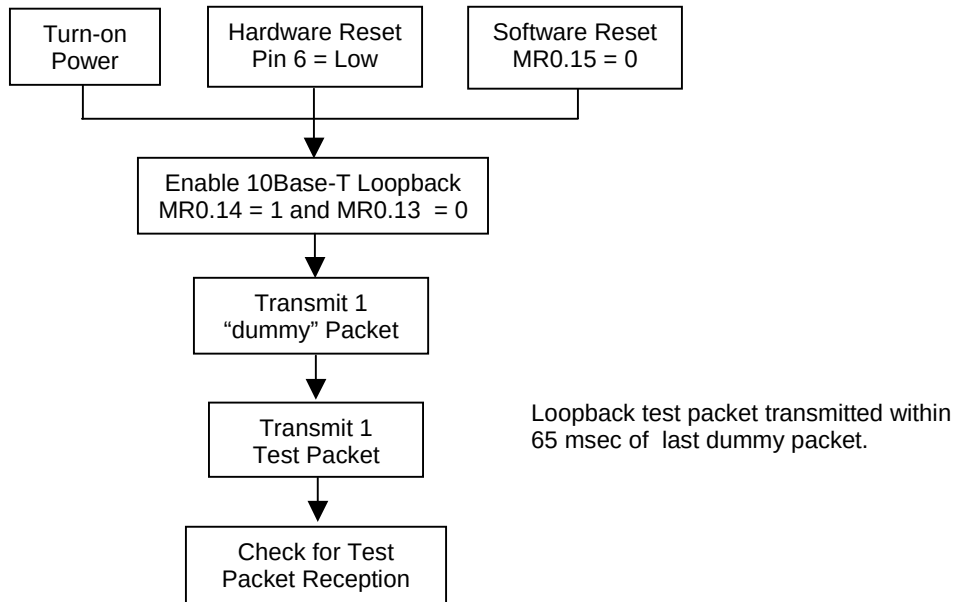


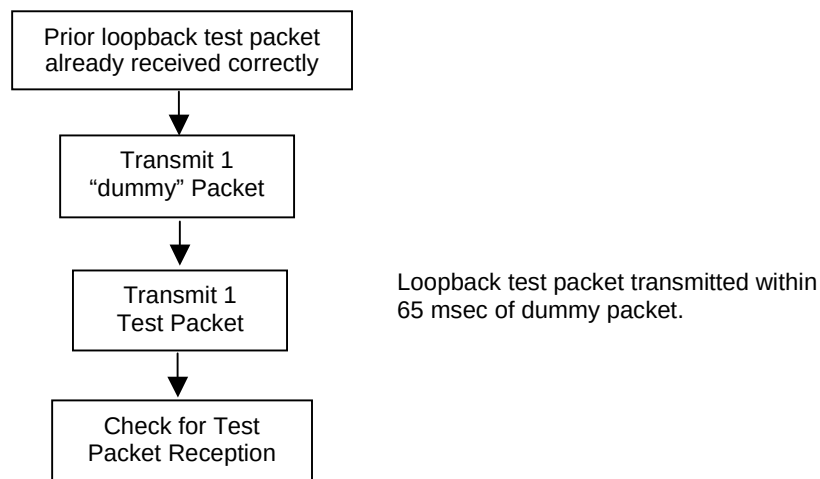
Figure 3 – MicroPHY 10Base-T Internal Loopback Path

INTERNAL LOOPBACK FLOWCHART

The following flowchart provides the sequence for receiving 10Base-T internal loopback data after a reset event:



The following flowchart provides the sequence for receiving 10Base-T internal loopback data after (more than 65 msec has expired since the reception of the last packet) the initial test packet has been received:



MII INTERFACE 10BASE-TX NATURAL LOOPBACK

Natural loopback is enabled by setting MII control register bit MR16.10 to a logic “1” and MR0.14, MR0.13 and MR0.8 are all logic “0”. Natural loopback is only a 10Base-T function. The 10Base-T natural loopback function is a carry over from the coaxial interface 10Base-2 and 10Base-5. These interfaces are half-duplex and the natural loopback function is used to test the PHY’s jabber detection circuitry. Natural loopback redirects the PHY’s transmitted data back to its receiver when no external network traffic is present.

The 10Base-T half duplex natural loopback operation behaves identical to the 10Base-T loopback function (MR0.14 = 1) when an external link is established with another 10Base-T PHY. Natural loopback does not work when 10Base-T link is not established. Initial packet corruption may occur after a hardware or software reset due to the Manchester encoder/decoder pipeline. Unlike internal loopback, the MicroPHY does not drop the first received packet in natural loopback mode.

10Base-T full duplex natural loopback operation is an invalid configuration. Additionally, enabling both natural loopback (setting MR16.10 to logic “1”) and loopback (setting MR0.14 to logic “1”) is an invalid configuration. These two invalid configurations are not supported and not recommended for use.

Figure 4 shows the 10Base-T half duplex natural loopback configuration.

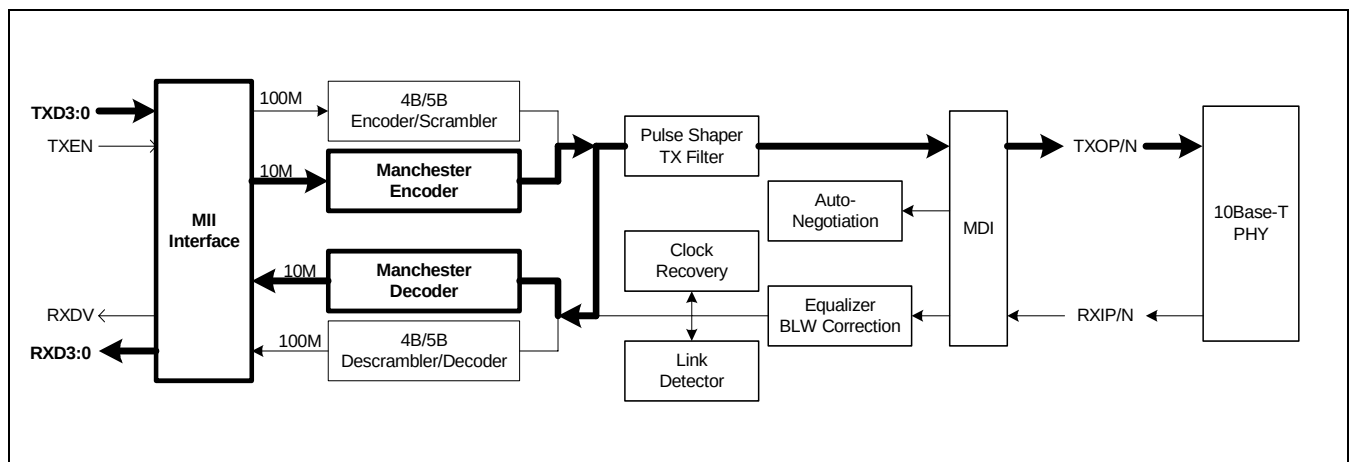


Figure 4 – MicroPHY 10Base-T Half Duplex Natural Loopback Path

MII INTERFACE EXTERNAL LOOPBACK

External loopback is performed using an external cable loopback plug. Figure 5 shows the external loopback configuration for 10Base-T.

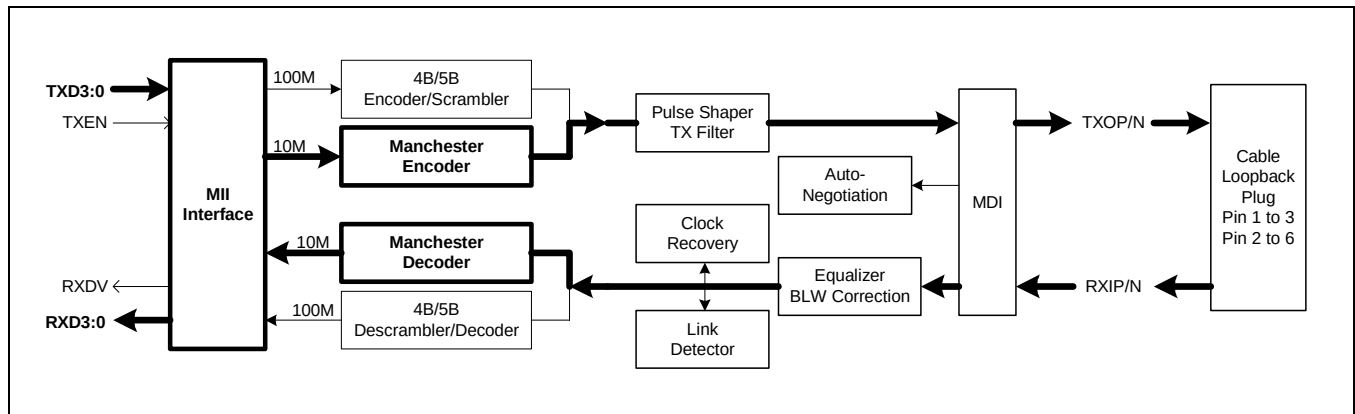


Figure 5 – MicroPHY External Loopback Path

There are no limitations on 100Base-TX external loopback operation. 10Base-T operation has the following two operational issues:

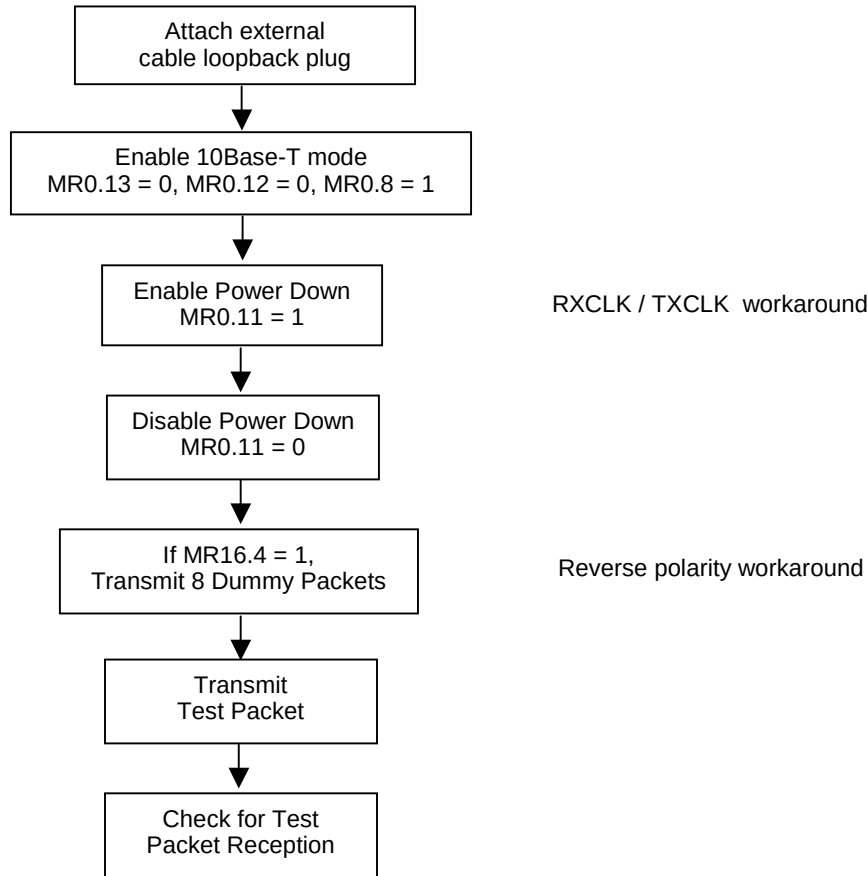
1. A reversed receive signal polarity requires eight packets to confirm the polarity reversal.
2. RXCLK and TXCLK may not be active upon switching to 10Base-T operation.

If the received signal polarity is reversed (reversed polarity bit MR16.4 is a logic “1”), eight packets must be received to confirm the signal polarity reversal. “Link up” is not asserted until confirmation of signal polarity is completed. Therefore, RXDV is not active during the reception of these eight packets (requiring transmission of 8 dummy packets). Transmission of eight dummy packets are not required if the receive signal polarity is positive (MR16.4 is a logic “0”).

Due to an internal timing problem resulting from the highly synchronized timing relationship between the transmitted and received signals when using the external cable loopback plug, the 10Base-T clock generator may not reset properly upon switching to 10Base-T operation. The 10Base-T clock generator resets properly when connected to a remote PHY due to the remote PHY’s delayed response in returning 10Base-T NLPs. The 10Base-T clock generator circuit provides the reference clock for RXCLK and TXCLK. Proper operation of the 10Base-T clock generator and subsequent RXCLK and TXCLK outputs can be guaranteed by performing a power down after switching to 10Base-T mode.

10BASE-T EXTERNAL LOOPBACK FLOWCHART

The following flowchart provides the sequence for receiving 10Base-T external loopback data:



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Teridian Semiconductor Corporation, 6440 Oak Canyon, Irvine, CA 92618-5201
(714) 508-8800, FAX: (714) 508-8877